Fundamentals of Power Electronics

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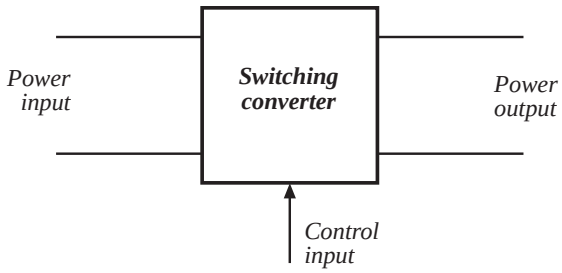
Chapter 1: Introduction

1.1. Introduction to power processing
1.2. Some applications of power electronics
1.3. Elements of power electronics
Summary of the course

1.1 Introduction to Power Processing



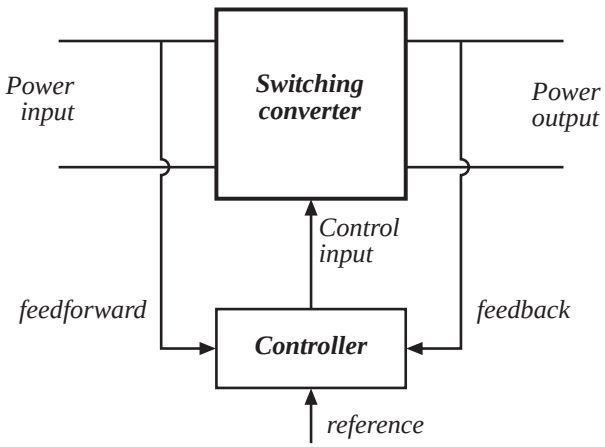
Dc-dc conversion: Change and control voltage magnitude

Ac-dc rectification: Possibly control dc voltage, ac current

Dc-ac inversion: Produce sinusoid of controllable magnitude and frequency

Ac-ac cycloconversion: Change and control voltage magnitude and frequency

Control is invariably required

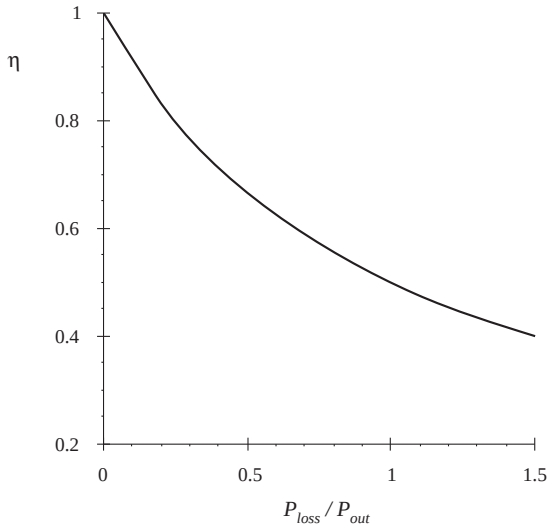


High efficiency is essential

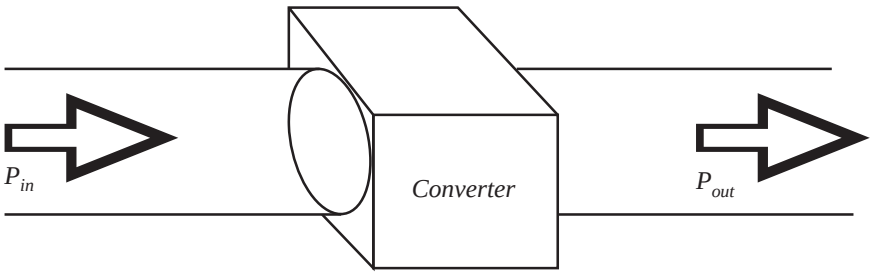
$$\eta = \frac{P_{out}}{P_{in}}$$

$$P_{loss} = P_{in} - P_{out} = P_{out}\left(\frac{1}{\eta} - 1\right)$$

- High efficiency leads to low power loss within converter
- Small size and reliable operation is then feasible
- Efficiency is a good measure of converter performance

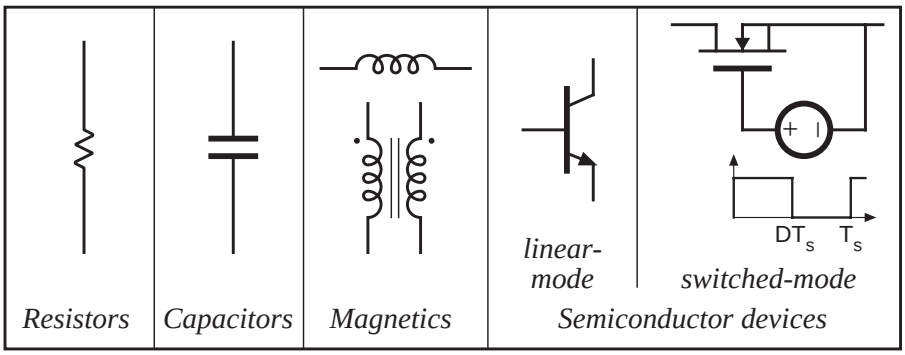


A high-efficiency converter

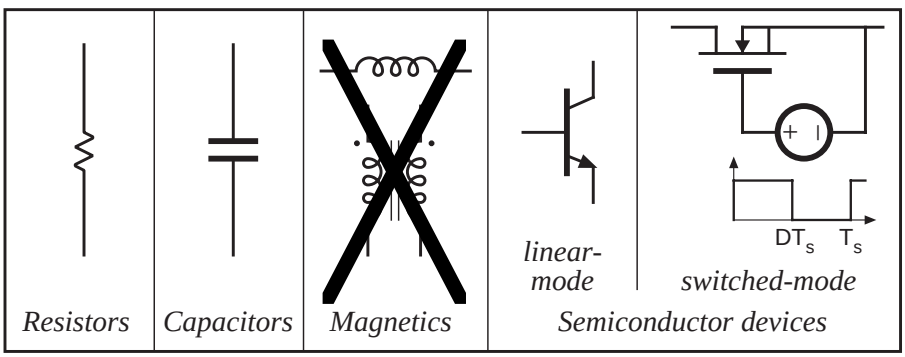


A goal of current converter technology is to construct converters of small size and weight, which process substantial power at high efficiency

Devices available to the circuit designer

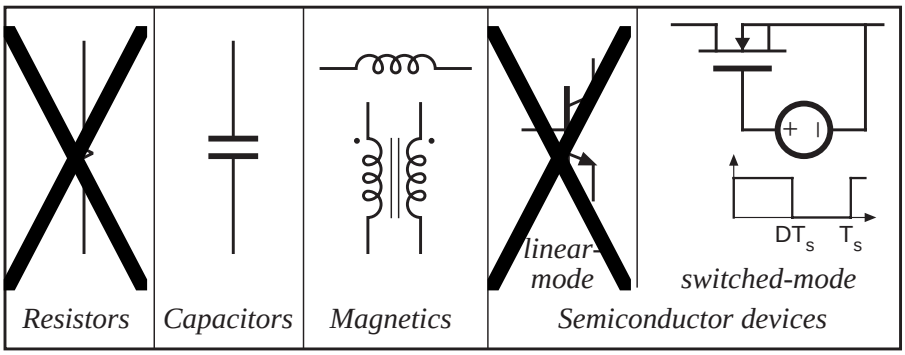


Devices available to the circuit designer



Signal processing: avoid magnetics

Devices available to the circuit designer



Power processing: avoid lossy elements

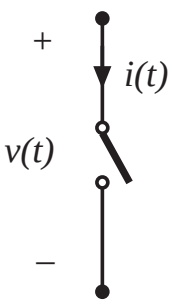
Power loss in an ideal switch

Switch closed: $v(t) = 0$

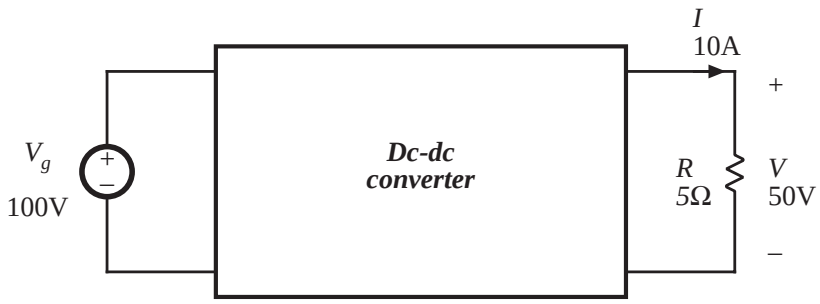
Switch open: $i(t) = 0$

In either event: $p(t) = v(t)\, i(t) = 0$

Ideal switch consumes zero power



A simple dc-dc converter example



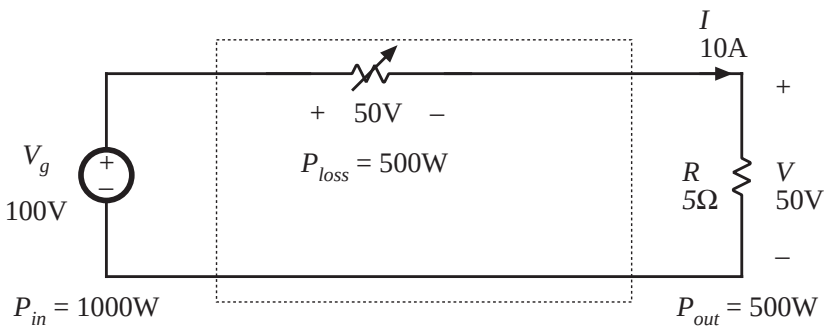
Input source: 100V

Output load: 50V, 10A, 500W

How can this converter be realized?

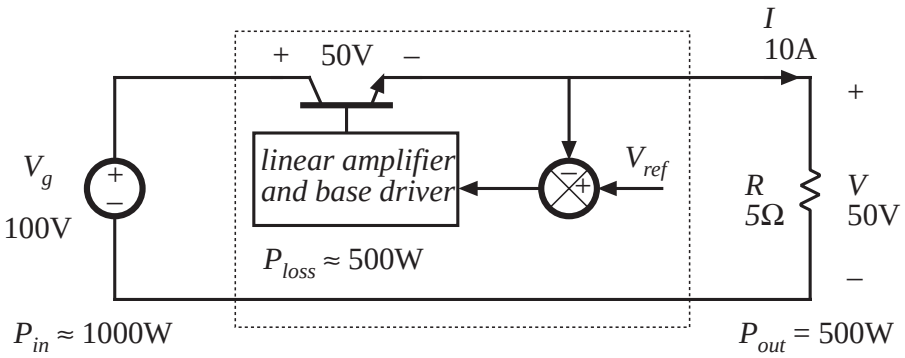
Dissipative realization

Resistive voltage divider

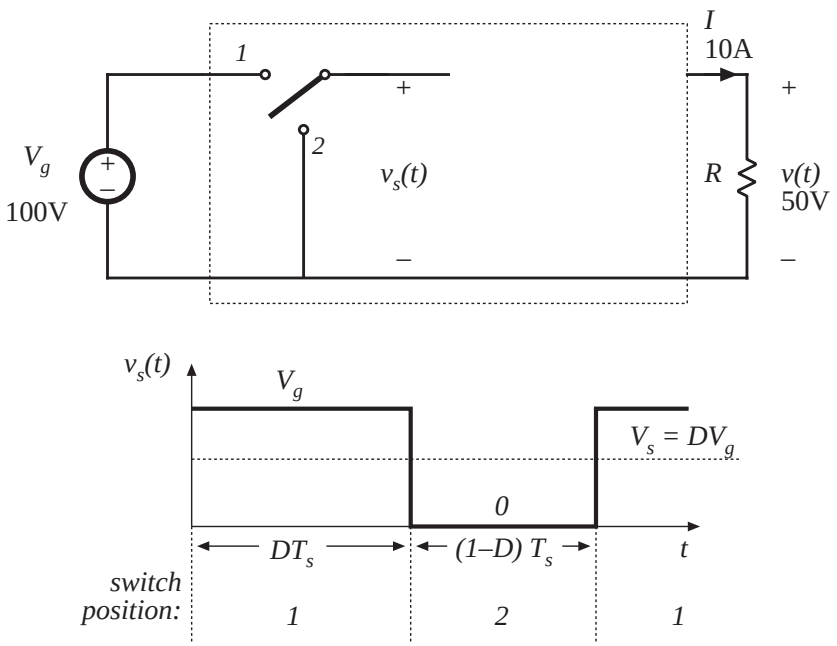


Dissipative realization

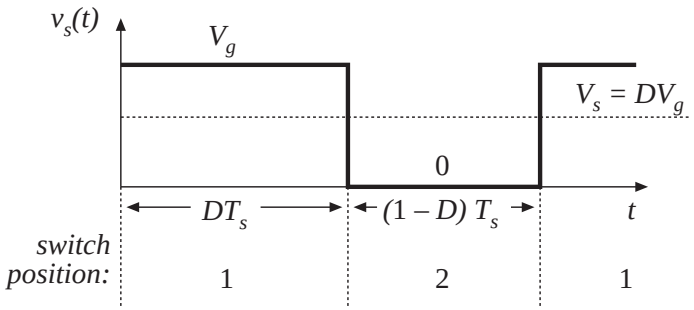
Series pass regulator: transistor operates in active region



Use of a SPDT switch



The switch changes the dc voltage level



D = switch duty cycle

$0 \le D \le 1$

T_s = switching period

f_s = switching frequency

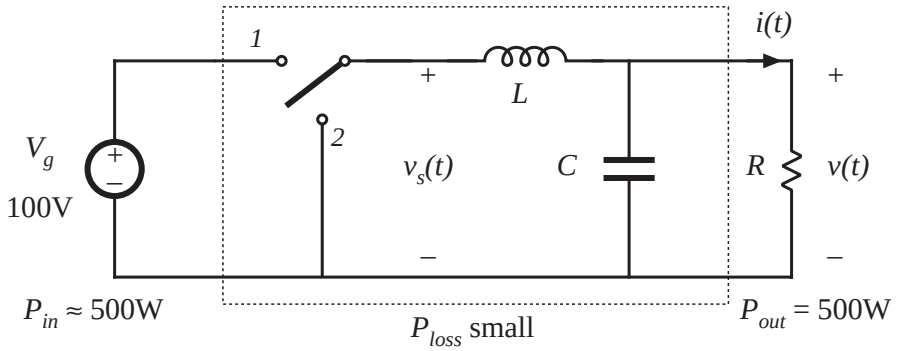
$= 1 / T_s$

DC component of $v_s(t)$ = average value:

$$V_s = \frac{1}{T_s}\int_0^{T_s} v_s(t)\,dt = DV_g$$

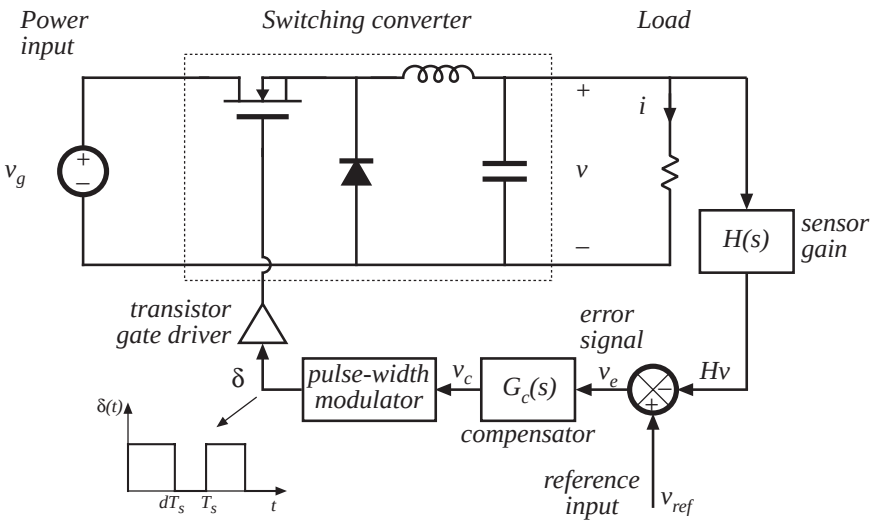
Addition of low pass filter

Addition of (ideally lossless) L-C low-pass filter, for removal of switching harmonics:

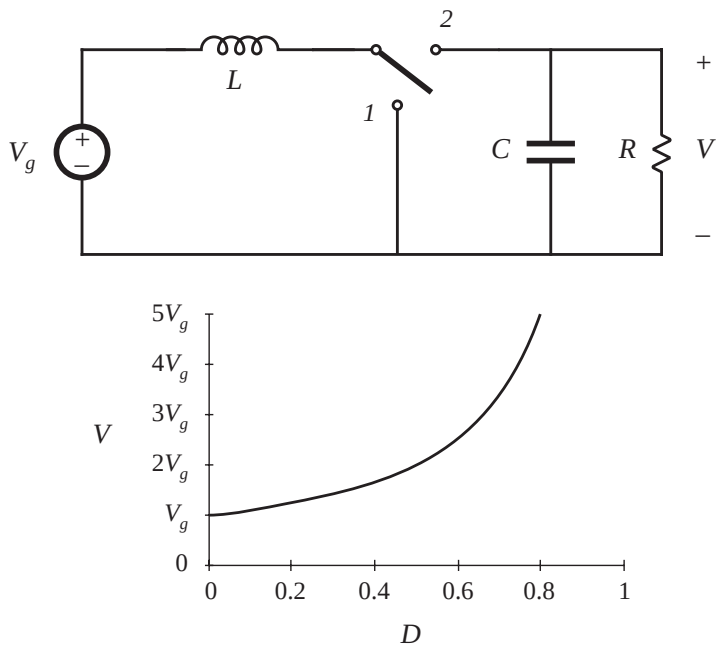


- Choose filter cutoff frequency f_0 much smaller than switching frequency f_s
- This circuit is known as the “buck converter”

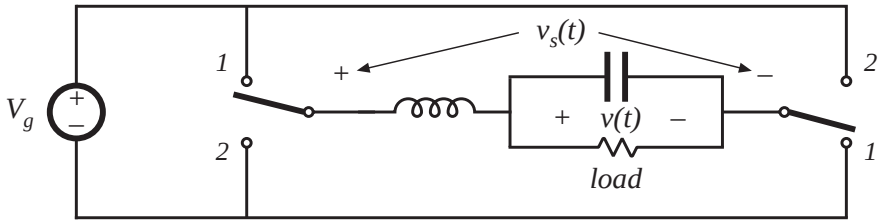
Addition of control system for regulation of output voltage

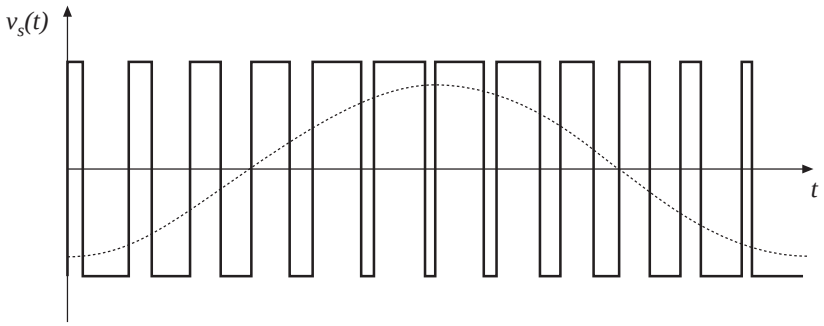


The boost converter



A single-phase inverter





"H-bridge"

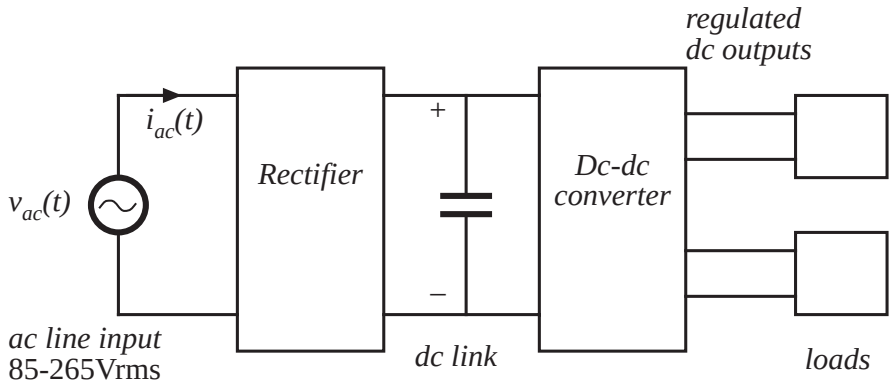
Modulate switch duty cycles to obtain sinusoidal low-frequency component

1.2 Several applications of power electronics

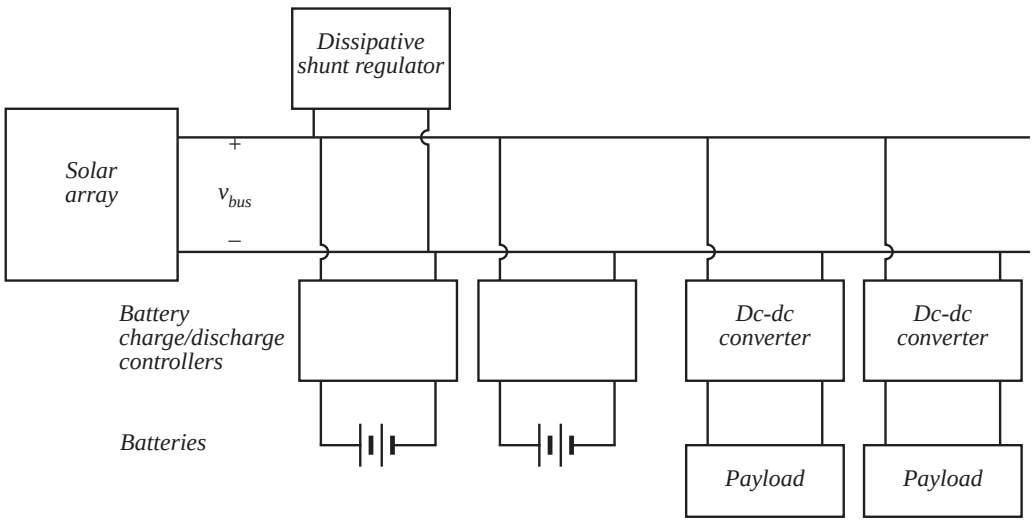
Power levels encountered in high-efficiency converters

- less than 1 W in battery-operated portable equipment
- tens, hundreds, or thousands of watts in power supplies for computers or office equipment
- kW to MW in variable-speed motor drives
- 1000 MW in rectifiers and inverters for utility dc transmission lines

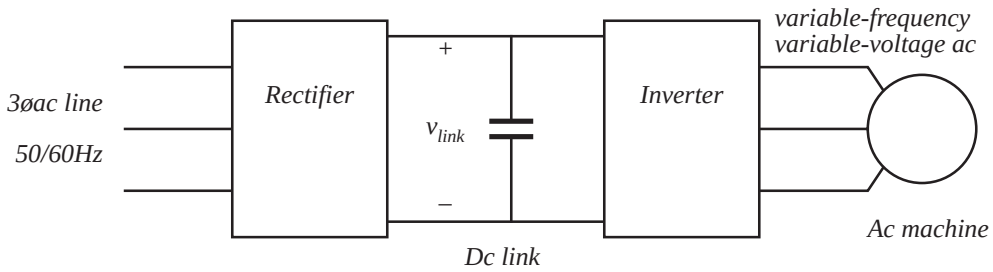
A computer power supply system



A spacecraft power system



A variable-speed ac motor drive system



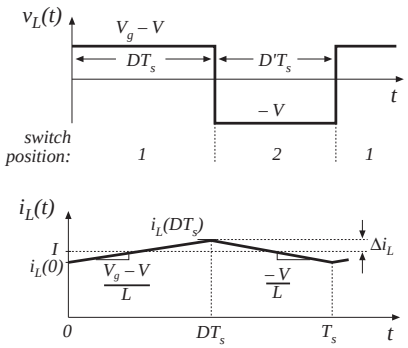
1.3 Elements of power electronics

Power electronics incorporates concepts from the fields of

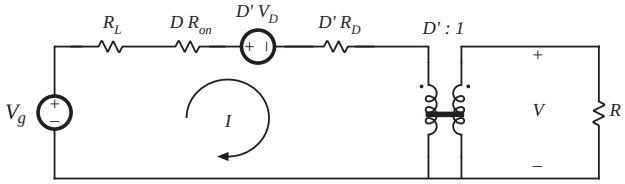
- analog circuits
- electronic devices
- control systems
- power systems
- magnetics
- electric machines
- numerical simulation

Part I. Converters in equilibrium

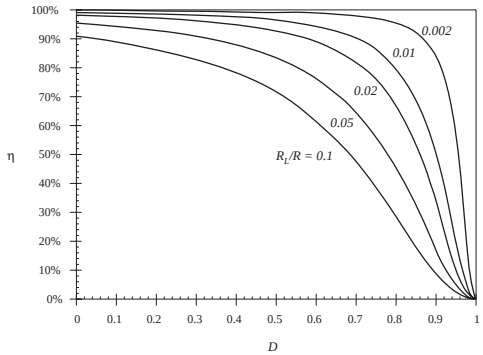
Inductor waveforms



Averaged equivalent circuit



Predicted efficiency

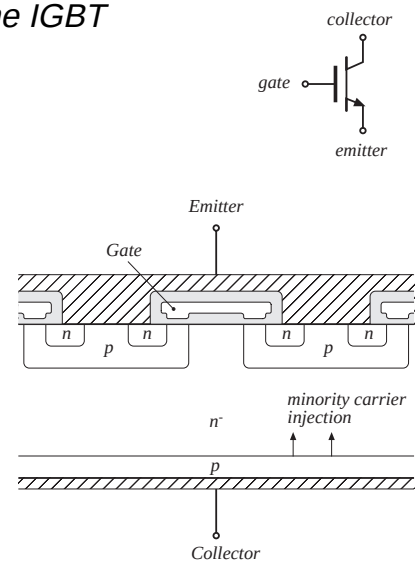


Discontinuous conduction mode

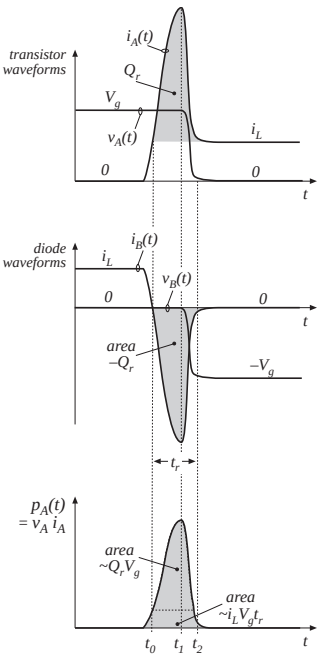
Transformer isolation

Switch realization: semiconductor devices

The IGBT



Switching loss

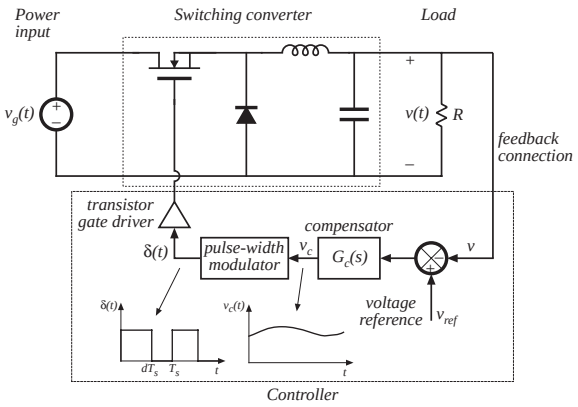


Part I. Converters in equilibrium

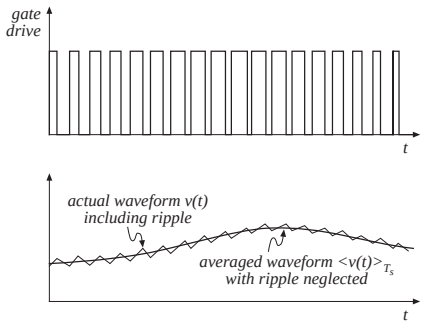
2. Principles of steady state converter analysis
3. Steady-state equivalent circuit modeling, losses, and efficiency
4. Switch realization
5. The discontinuous conduction mode
6. Converter circuits

Part II. Converter dynamics and control

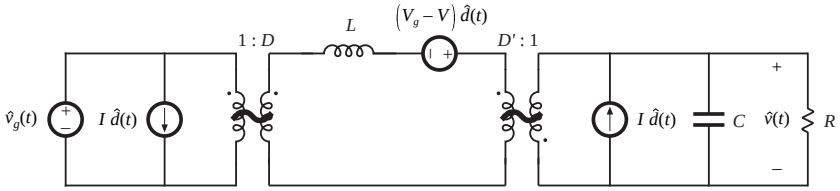
Closed-loop converter system



Averaging the waveforms



Small-signal averaged equivalent circuit

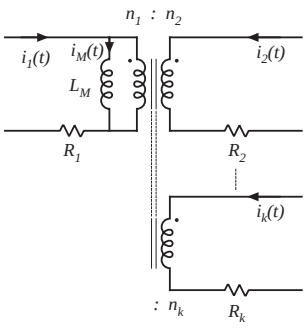


Part II. Converter dynamics and control

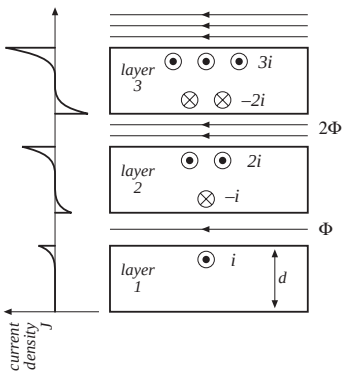
7. Ac modeling
8. Converter transfer functions
9. Controller design
10. Ac and dc equivalent circuit modeling of the discontinuous conduction mode
11. Current-programmed control

Part III. Magnetics

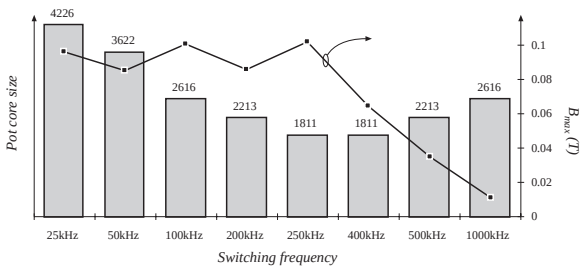
transformer design



the proximity effect



transformer size vs. switching frequency

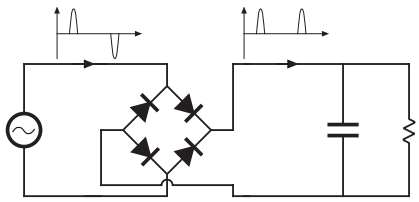


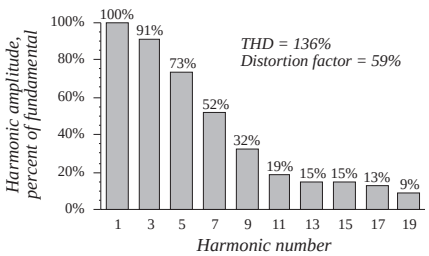
Part III. Magnetics

12. Basic magnetics theory
13. Filter inductor design
14. Transformer design

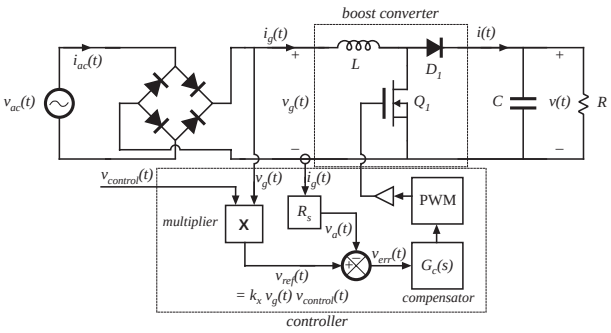
Part IV. Modern rectifiers,
and power system harmonics

Pollution of power system by rectifier current harmonics

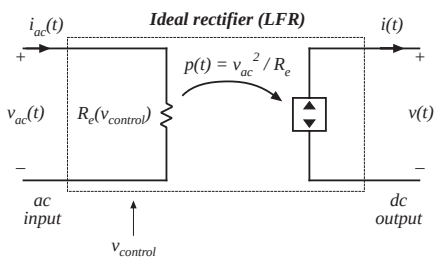




A low-harmonic rectifier system



Model of the ideal rectifier

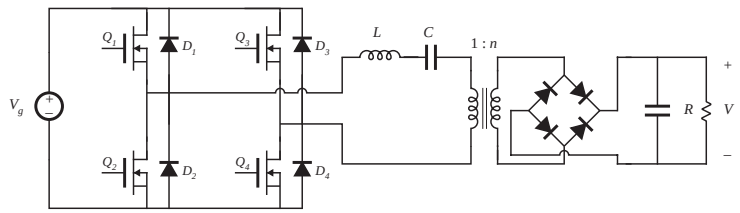


Part IV. Modern rectifiers,
and power system harmonics

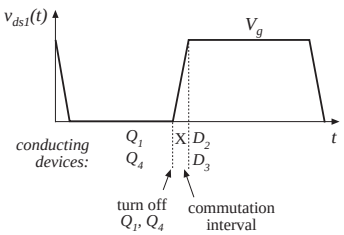
15. Power and harmonics in nonsinusoidal systems
16. Line-commutated rectifiers
17. The ideal rectifier
18. Low harmonic rectifier modeling and control

Part V. Resonant converters

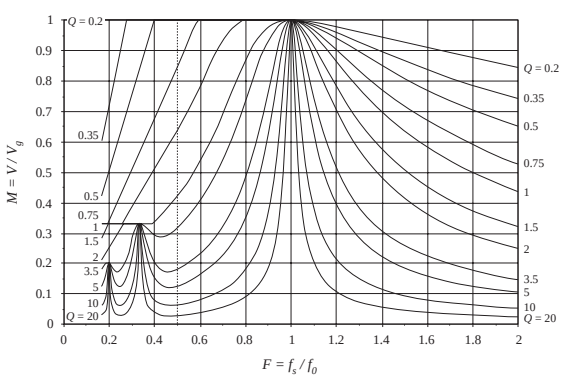
The series resonant converter



Zero voltage switching



Dc characteristics



Part V. Resonant converters

19. Resonant conversion
20. Quasi-resonant converters

Chapter 2
Principles of Steady-State Converter Analysis

2.1. Introduction

2.2. Inductor volt-second balance, capacitor charge balance, and the small ripple approximation

2.3. Boost converter example

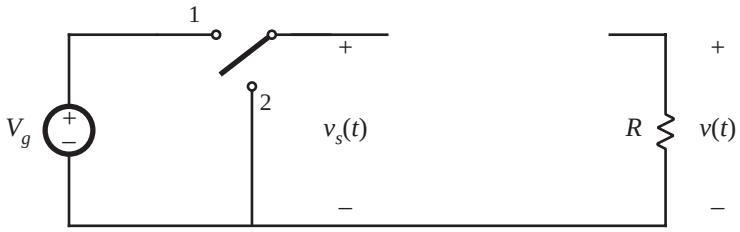
2.4. Cuk converter example

2.5. Estimating the ripple in converters containing two-pole low-pass filters

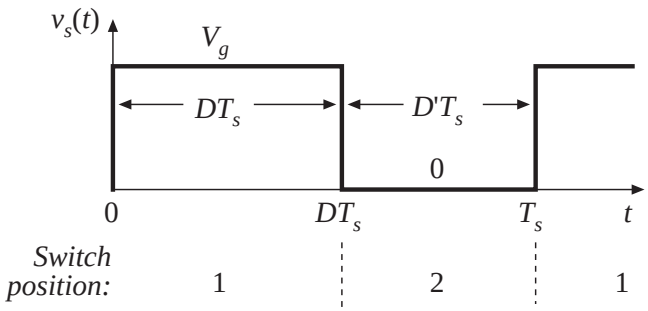
2.6. Summary of key points

2.1 Introduction
Buck converter

SPDT switch changes dc component



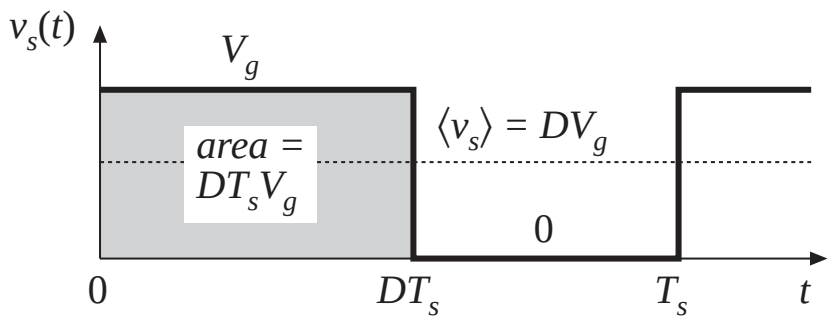
Switch output voltage waveform



Duty cycle D:
$0 \le D \le 1$

complement D':
$D' = 1 - D$

Dc component of switch output voltage

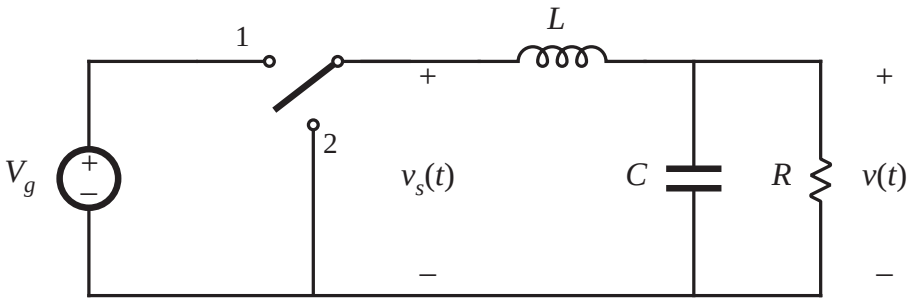


Fourier analysis: Dc component = average value

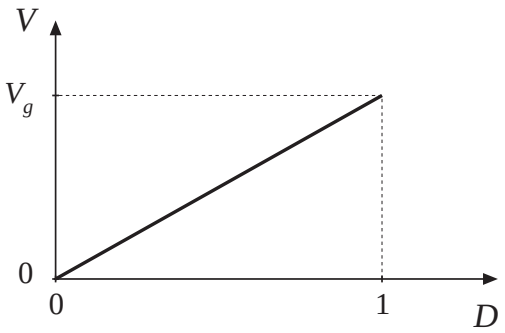
$$\langle v_s \rangle = \frac{1}{T_s}\int_0^{T_s} v_s(t)\,dt$$

$$\langle v_s \rangle = \frac{1}{T_s}\,(DT_sV_g) = DV_g$$

Insertion of low-pass filter to remove switching harmonics and pass only dc component

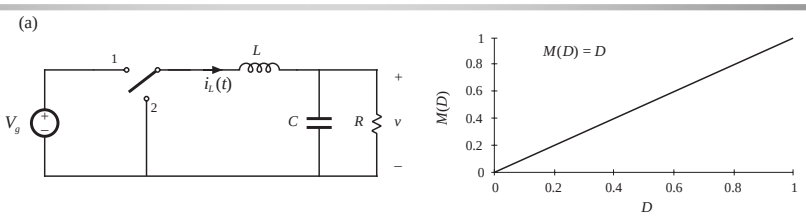


$$v \approx \langle v_s \rangle = DV_g$$

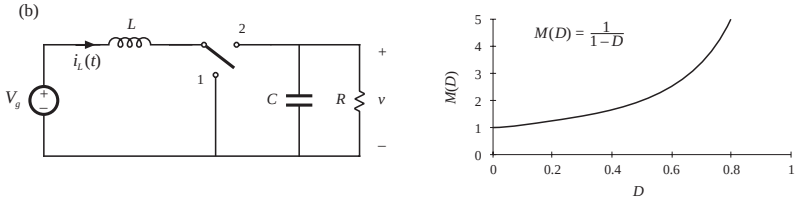


Three basic dc-dc converters

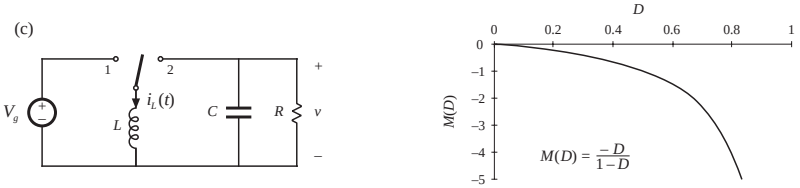
Buck



Boost



Buck-boost



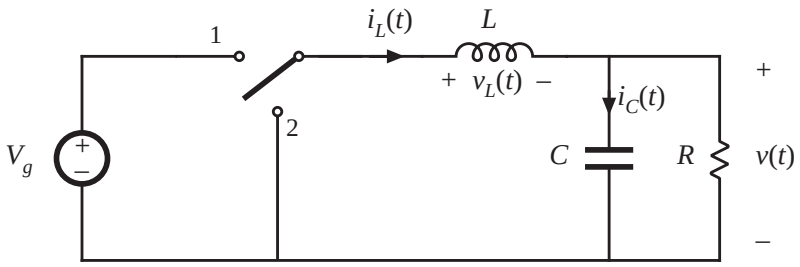
Objectives of this chapter

- Develop techniques for easily determining output voltage of an arbitrary converter circuit
- Derive the principles of *inductor volt-second balance* and *capacitor charge (amp-second) balance*
- Introduce the key *small ripple approximation*
- Develop simple methods for selecting filter element values
- Illustrate via examples

2.2. Inductor volt-second balance, capacitor charge balance, and the small ripple approximation

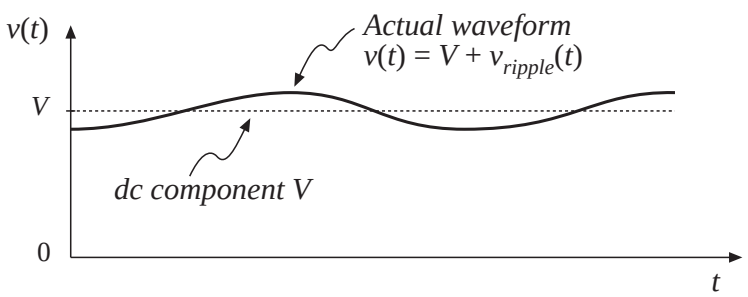
Actual output voltage waveform, buck converter

Buck converter containing practical low-pass filter



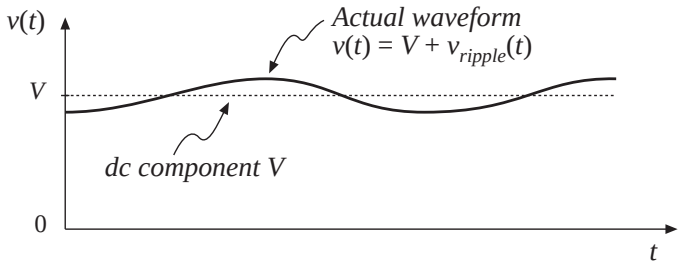
Actual output voltage waveform

$v(t) = V + v_{ripple}(t)$



The small ripple approximation

$$v(t) = V + v_{ripple}(t)$$

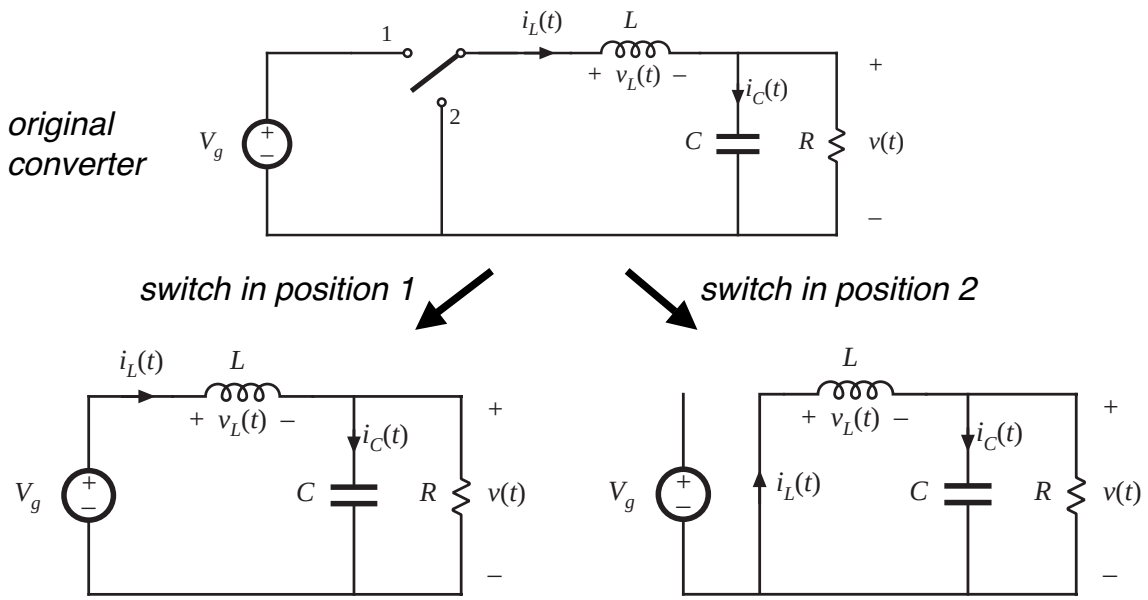


In a well-designed converter, the output voltage ripple is small. Hence, the waveforms can be easily determined by ignoring the ripple:

$$\left\| v_{ripple} \right\| \ll V$$

$$v(t) \approx V$$

Buck converter analysis: inductor current waveform



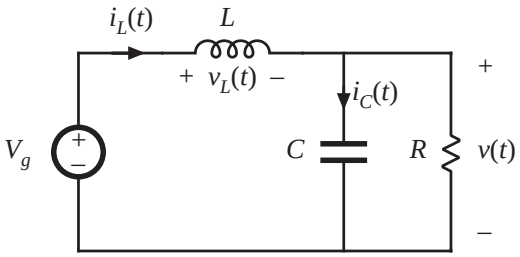
Inductor voltage and current
Subinterval 1: switch in position 1

Inductor voltage

$$v_L = V_g - v(t)$$

Small ripple approximation:

$$v_L \approx V_g - V$$



Knowing the inductor voltage, we can now find the inductor current via

$$v_L(t) = L \frac{di_L(t)}{dt}$$

Solve for the slope:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} \approx \frac{V_g - V}{L}$$

⇒ *The inductor current changes with an essentially constant slope*

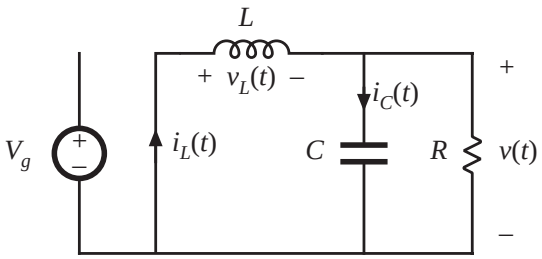
Inductor voltage and current
Subinterval 2: switch in position 2

Inductor voltage

$$v_L(t) = -v(t)$$

Small ripple approximation:

$$v_L(t) \approx -V$$



Knowing the inductor voltage, we can again find the inductor current via

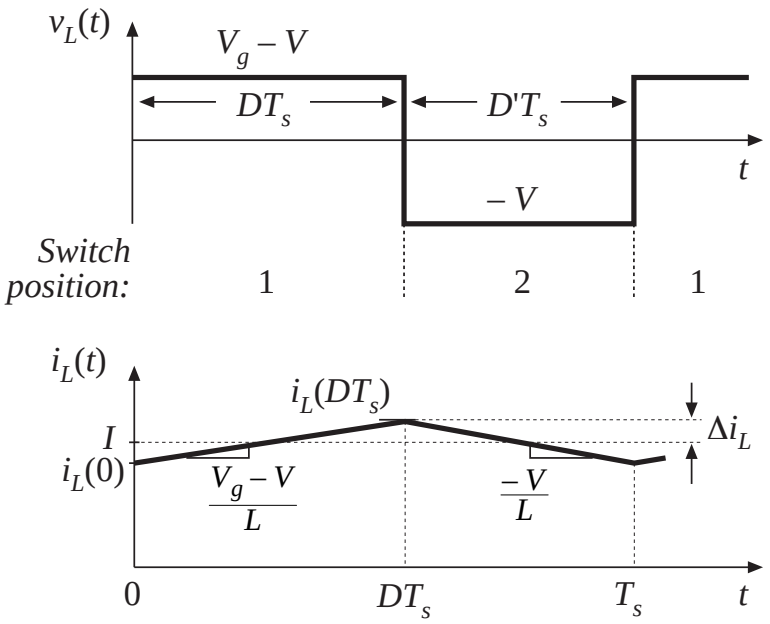
$$v_L(t) = L \frac{di_L(t)}{dt}$$

Solve for the slope:

$$\frac{di_L(t)}{dt} \approx -\frac{V}{L}$$

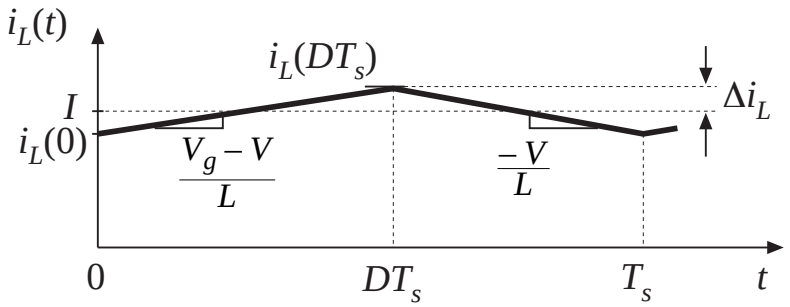
⇒ *The inductor current changes with an essentially constant slope*

Inductor voltage and current waveforms



$$v_L(t) = L\,\frac{di_L(t)}{dt}$$

Determination of inductor current ripple magnitude

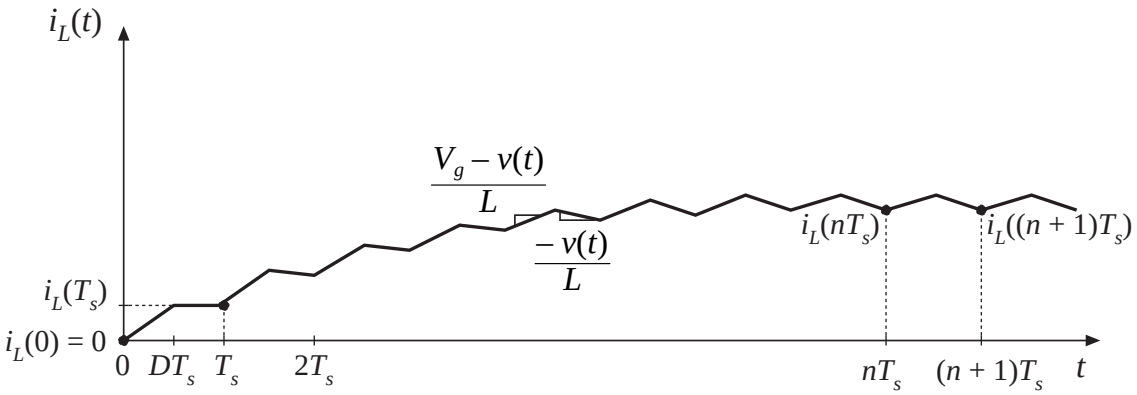


(*change in* i_L) = (*slope*)(*length of subinterval*)

$$\left(2\Delta i_L\right) = \left(\frac{V_g - V}{L}\right)\left(DT_s\right)$$

$$\Rightarrow \qquad \Delta i_L = \frac{V_g - V}{2L}\,DT_s \qquad\qquad L = \frac{V_g - V}{2\Delta i_L}\,DT_s$$

Inductor current waveform during turn-on transient



When the converter operates in equilibrium:

$$i_L((n+1)T_s) = i_L(nT_s)$$

The principle of inductor volt-second balance: Derivation

Inductor defining relation:

$$v_L(t) = L\,\frac{di_L(t)}{dt}$$

Integrate over one complete switching period:

$$i_L(T_s) - i_L(0) = \frac{1}{L}\int_0^{T_s} v_L(t)\,dt$$

In periodic steady state, the net change in inductor current is zero:

$$0 = \int_0^{T_s} v_L(t)\,dt$$

Hence, the total area (or volt-seconds) under the inductor voltage waveform is zero whenever the converter operates in steady state.

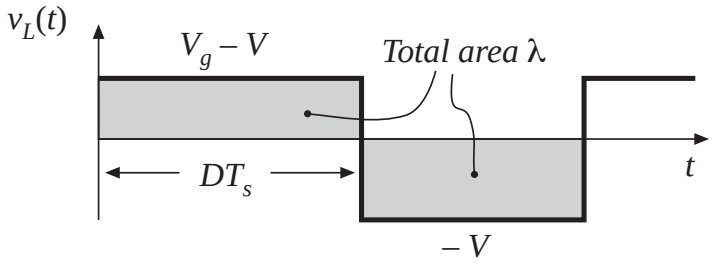
An equivalent form:

$$0 = \frac{1}{T_s}\int_0^{T_s} v_L(t)\,dt = \left\langle v_L \right\rangle$$

The average inductor voltage is zero in steady state.

Inductor volt-second balance: Buck converter example

Inductor voltage waveform, previously derived:



Integral of voltage waveform is area of rectangles:

$$\lambda = \int_0^{T_s} v_L(t)\, dt = (V_g - V)(DT_s) + (-V)(D'T_s)$$

Average voltage is

$$\langle v_L \rangle = \frac{\lambda}{T_s} = D(V_g - V) + D'(-V)$$

Equate to zero and solve for *V:*

$$0 = DV_g - (D + D')V = DV_g - V \qquad \Rightarrow \qquad V = DV_g$$

The principle of capacitor charge balance: Derivation

Capacitor defining relation:

$$i_C(t) = C\,\frac{dv_C(t)}{dt}$$

Integrate over one complete switching period:

$$v_C(T_s) - v_C(0) = \frac{1}{C}\int_0^{T_s} i_C(t)\, dt$$

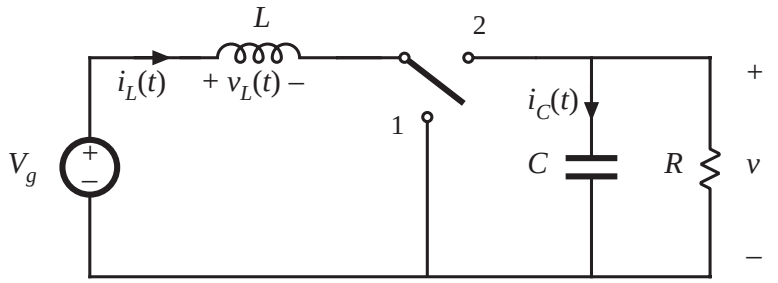
In periodic steady state, the net change in capacitor voltage is zero:

$$0 = \frac{1}{T_s}\int_0^{T_s} i_C(t)\, dt = \langle i_C \rangle$$

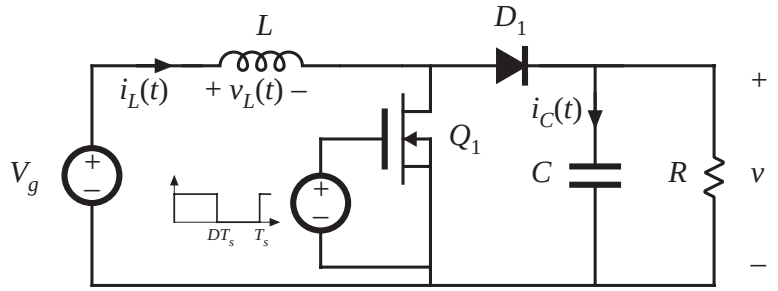
Hence, the total area (or charge) under the capacitor current waveform is zero whenever the converter operates in steady state. The average capacitor current is then zero.

2.3 Boost converter example

Boost converter with ideal switch

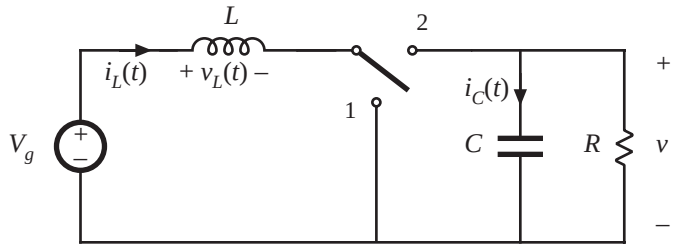


Realization using power MOSFET and diode

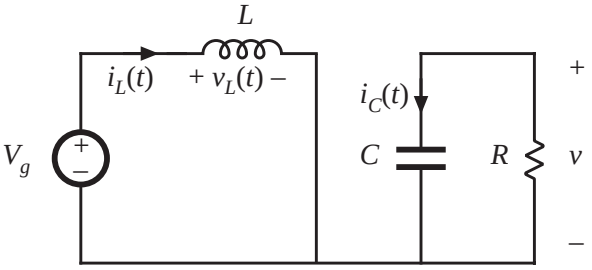


Boost converter analysis

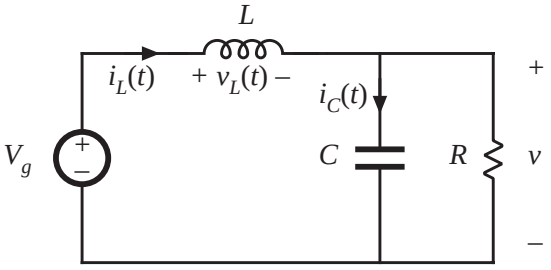
original converter



switch in position 1



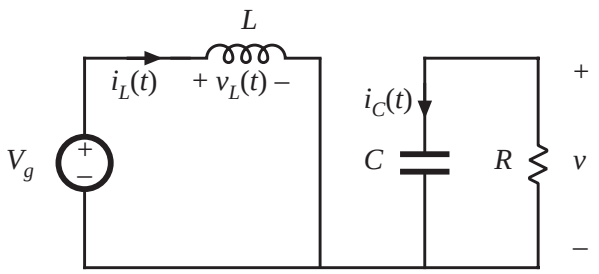
switch in position 2



Subinterval 1: switch in position 1

Inductor voltage and capacitor current

$$v_L = V_g$$
$$i_C = -v / R$$



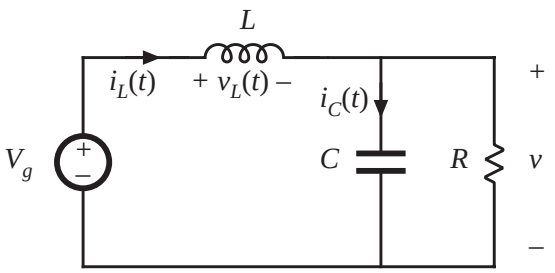
Small ripple approximation:

$$v_L = V_g$$
$$i_C = -V / R$$

Subinterval 2: switch in position 2

Inductor voltage and capacitor current

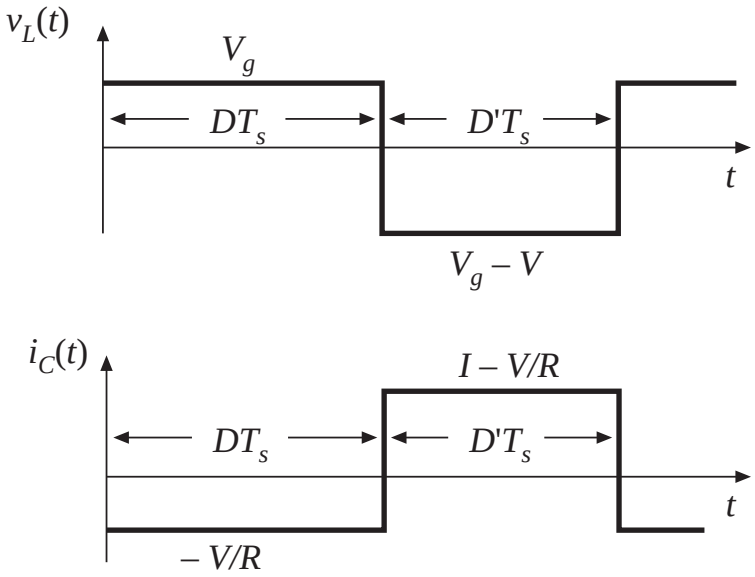
$$v_L = V_g - v$$
$$i_C = i_L - v / R$$



Small ripple approximation:

$$v_L = V_g - V$$
$$i_C = I - V / R$$

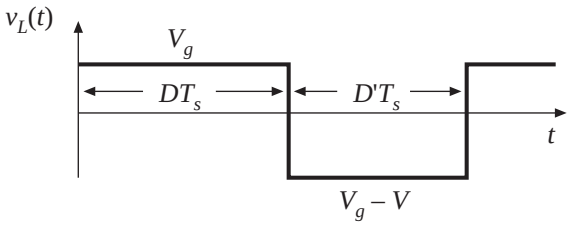
Inductor voltage and capacitor current waveforms



Inductor volt-second balance

Net volt-seconds applied to inductor over one switching period:

$$\int_0^{T_s} v_L(t)\, dt = (V_g)\, DT_s + (V_g - V)\, D'T_s$$



Equate to zero and collect terms:

$$V_g\,(D + D') - V\,D' = 0$$

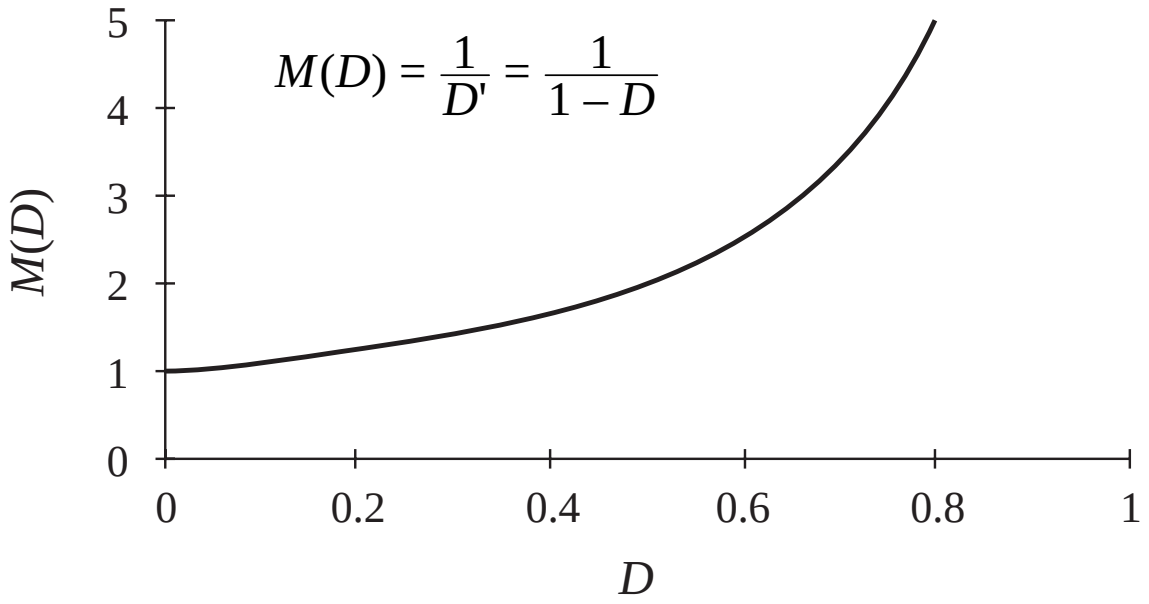
Solve for V:

$$V = \frac{V_g}{D'}$$

The voltage conversion ratio is therefore

$$M(D) = \frac{V}{V_g} = \frac{1}{D'} = \frac{1}{1 - D}$$

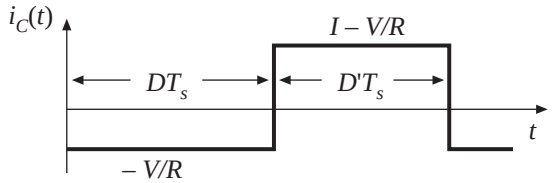
Conversion ratio *M(D)* of the boost converter



Determination of inductor current dc component

Capacitor charge balance:

$$\int_0^{T_s} i_C(t)\, dt = \left(-\frac{V}{R}\right) DT_s + \left(I - \frac{V}{R}\right) D'T_s$$



Collect terms and equate to zero:

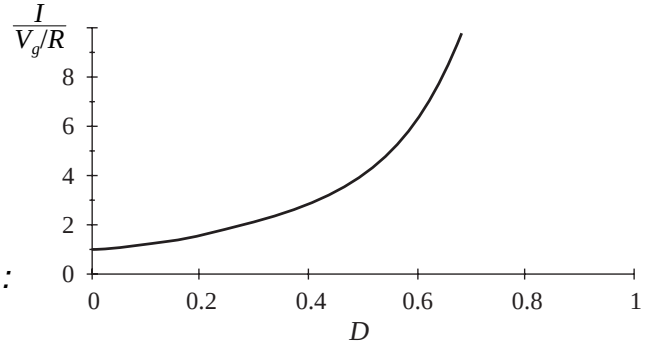
$$-\frac{V}{R}(D + D') + I\,D' = 0$$

Solve for *I:*

$$I = \frac{V}{D'\,R}$$

Eliminate *V* to express in terms of V_g:

$$I = \frac{V_g}{D'^2\,R}$$



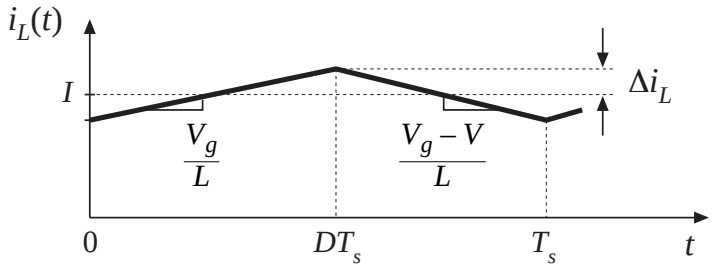
Determination of inductor current ripple

Inductor current slope during subinterval 1:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g}{L}$$

Inductor current slope during subinterval 2:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g - V}{L}$$



Change in inductor current during subinterval 1 is *(slope) (length of subinterval):*

$$2\Delta i_L = \frac{V_g}{L} DT_s$$

Solve for peak ripple:

$$\Delta i_L = \frac{V_g}{2L} DT_s$$

- Choose *L* such that desired ripple magnitude is obtained

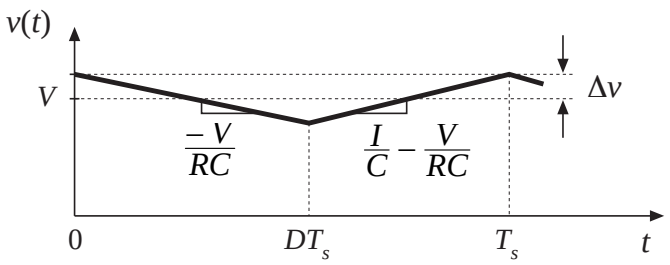
Determination of capacitor voltage ripple

Capacitor voltage slope during subinterval 1:

$$\frac{dv_C(t)}{dt} = \frac{i_C(t)}{C} = \frac{-V}{RC}$$

Capacitor voltage slope during subinterval 2:

$$\frac{dv_C(t)}{dt} = \frac{i_C(t)}{C} = \frac{I}{C} - \frac{V}{RC}$$



Change in capacitor voltage during subinterval 1 is *(slope) (length of subinterval):*

$$-2\Delta v = \frac{-V}{RC} DT_s$$

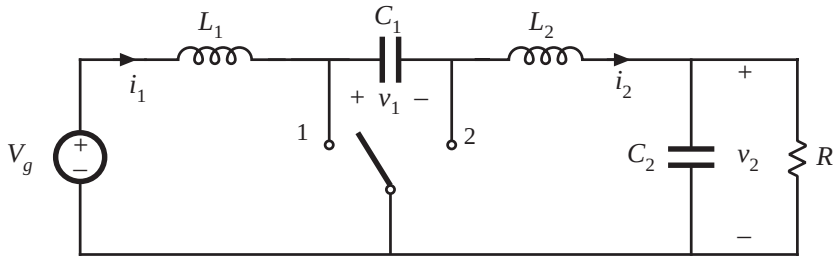
Solve for peak ripple:

$$\Delta v = \frac{V}{2RC} DT_s$$

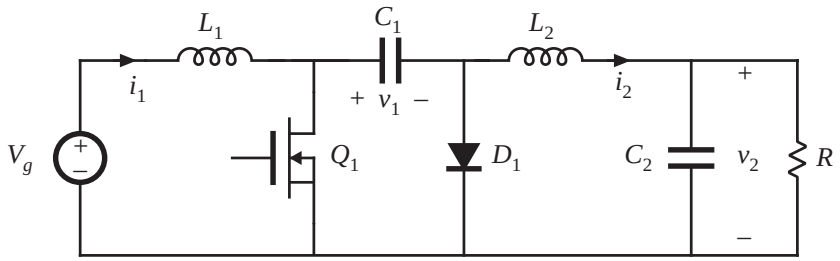
- Choose *C* such that desired voltage ripple magnitude is obtained
- In practice, capacitor *equivalent series resistance* (esr) leads to increased voltage ripple

2.4 Cuk converter example

Cuk converter, with ideal switch



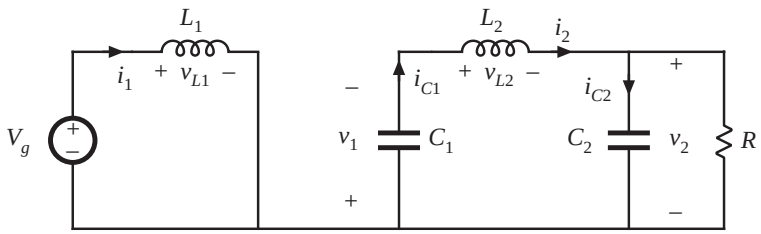
Cuk converter: practical realization using MOSFET and diode



Cuk converter circuit
with switch in positions 1 and 2

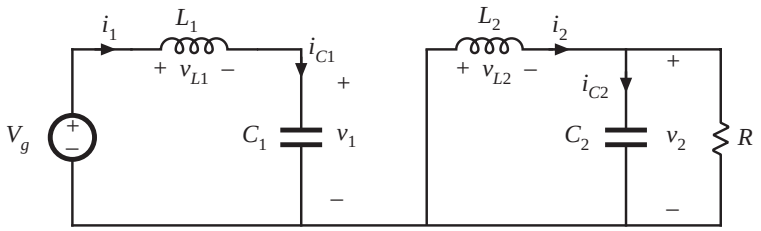
Switch in position 1: MOSFET conducts

Capacitor C_1 releases energy to output



Switch in position 2: diode conducts

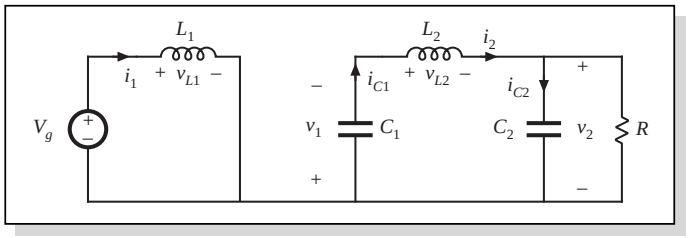
Capacitor C_1 is charged from input



Waveforms during subinterval 1
MOSFET conduction interval

Inductor voltages and capacitor currents:

$$v_{L1} = V_g$$
$$v_{L2} = -v_1 - v_2$$
$$i_{C1} = i_2$$
$$i_{C2} = i_2 - \frac{v_2}{R}$$



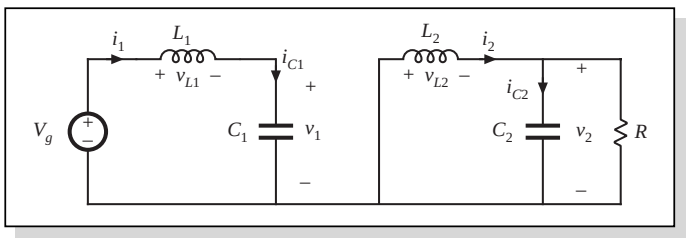
Small ripple approximation for subinterval 1:

$$v_{L1} = V_g$$
$$v_{L2} = -V_1 - V_2$$
$$i_{C1} = I_2$$
$$i_{C2} = I_2 - \frac{V_2}{R}$$

Waveforms during subinterval 2
Diode conduction interval

Inductor voltages and capacitor currents:

$$v_{L1} = V_g - v_1$$
$$v_{L2} = -v_2$$
$$i_{C1} = i_1$$
$$i_{C2} = i_2 - \frac{v_2}{R}$$



Small ripple approximation for subinterval 2:

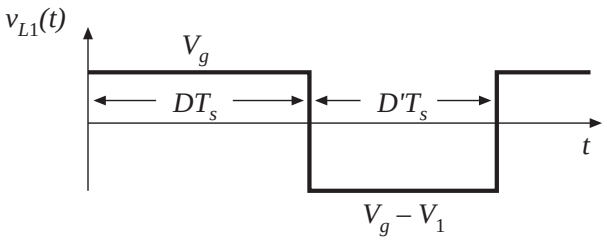
$$v_{L1} = V_g - V_1$$
$$v_{L2} = -V_2$$
$$i_{C1} = I_1$$
$$i_{C2} = I_2 - \frac{V_2}{R}$$

Equate average values to zero

The principles of inductor volt-second and capacitor charge balance state that the average values of the periodic inductor voltage and capacitor current waveforms are zero, when the converter operates in steady state. Hence, to determine the steady-state conditions in the converter, let us sketch the inductor voltage and capacitor current waveforms, and equate their average values to zero.

Waveforms:

Inductor voltage $v_{L1}(t)$

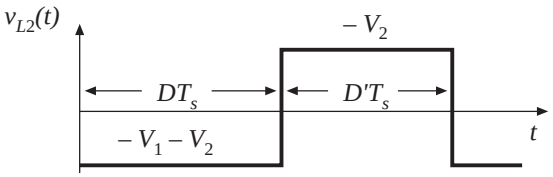


Volt-second balance on L_1:

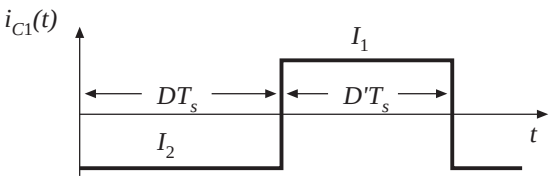
$$\langle v_{L1} \rangle = DV_g + D'(V_g - V_1) = 0$$

Equate average values to zero

Inductor L_2 voltage



Capacitor C_1 current

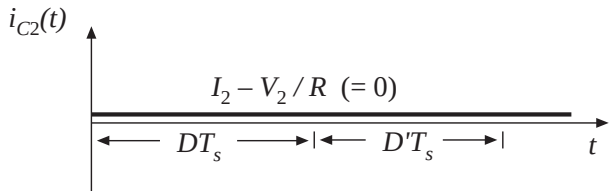


Average the waveforms:

$$\langle v_{L2} \rangle = D(-V_1 - V_2) + D'(-V_2) = 0$$
$$\langle i_{C1} \rangle = DI_2 + D'I_1 = 0$$

Equate average values to zero

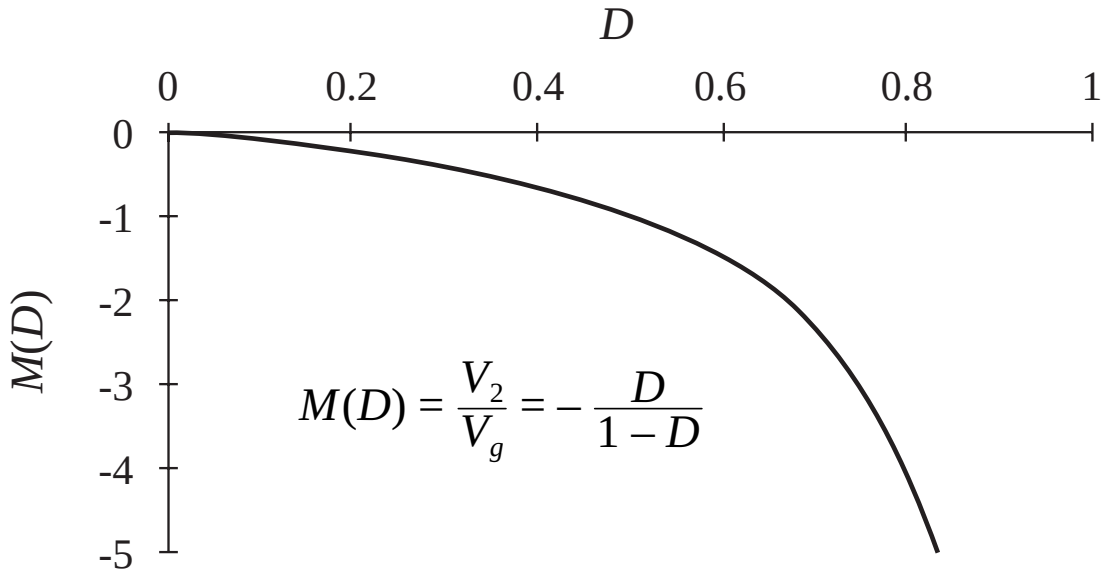
Capacitor current $i_{C2}(t)$ waveform



$$\left\langle i_{C2} \right\rangle = I_2 - \frac{V_2}{R} = 0$$

Note: during both subintervals, the capacitor current i_{C2} is equal to the difference between the inductor current i_2 and the load current V_2/R. When ripple is neglected, i_{C2} is constant and equal to zero.

Cuk converter conversion ratio $M = V / V_g$



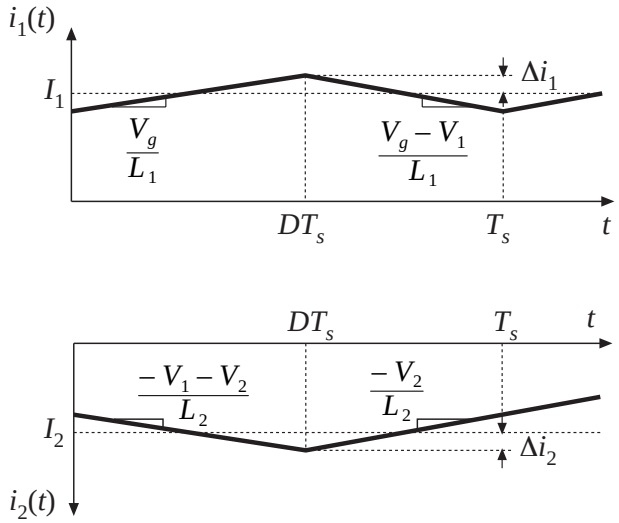
Inductor current waveforms

Interval 1 slopes, using small ripple approximation:

$$\frac{di_1(t)}{dt} = \frac{v_{L1}(t)}{L_1} = \frac{V_g}{L_1}$$
$$\frac{di_2(t)}{dt} = \frac{v_{L2}(t)}{L_2} = \frac{-V_1 - V_2}{L_2}$$

Interval 2 slopes:

$$\frac{di_1(t)}{dt} = \frac{v_{L1}(t)}{L_1} = \frac{V_g - V_1}{L_1}$$
$$\frac{di_2(t)}{dt} = \frac{v_{L2}(t)}{L_2} = \frac{-V_2}{L_2}$$



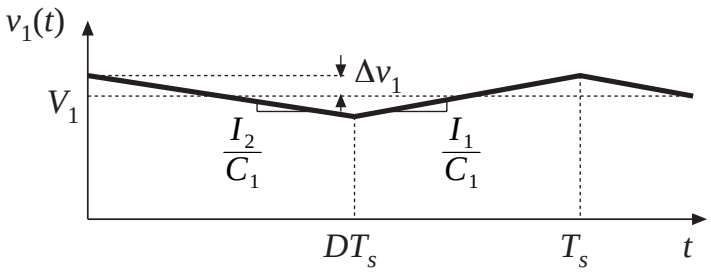
Capacitor C_1 waveform

Subinterval 1:

$$\frac{dv_1(t)}{dt} = \frac{i_{C1}(t)}{C_1} = \frac{I_2}{C_1}$$

Subinterval 2:

$$\frac{dv_1(t)}{dt} = \frac{i_{C1}(t)}{C_1} = \frac{I_1}{C_1}$$



Ripple magnitudes

Analysis results

$$\Delta i_1 = \frac{V_g D T_s}{2 L_1}$$

$$\Delta i_2 = \frac{V_1 + V_2}{2 L_2} D T_s$$

$$\Delta v_1 = \frac{-I_2 D T_s}{2 C_1}$$

Use dc converter solution to simplify:

$$\Delta i_1 = \frac{V_g D T_s}{2 L_1}$$

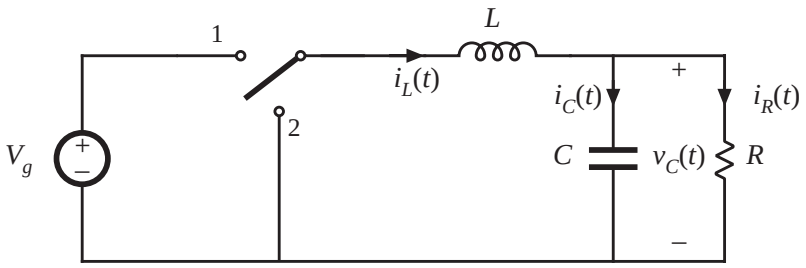
$$\Delta i_2 = \frac{V_g D T_s}{2 L_2}$$

$$\Delta v_1 = \frac{V_g D^2 T_s}{2 D' R C_1}$$

Q: How large is the output voltage ripple?

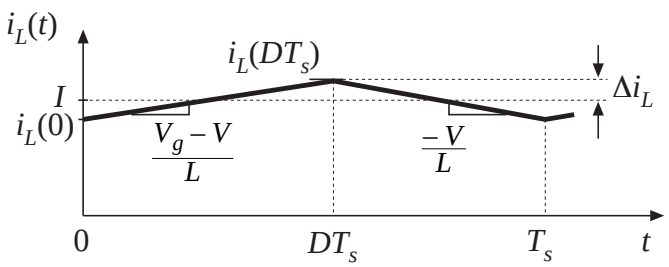
2.5 Estimating ripple in converters containing two-pole low-pass filters

Buck converter example: Determine output voltage ripple



Inductor current waveform.

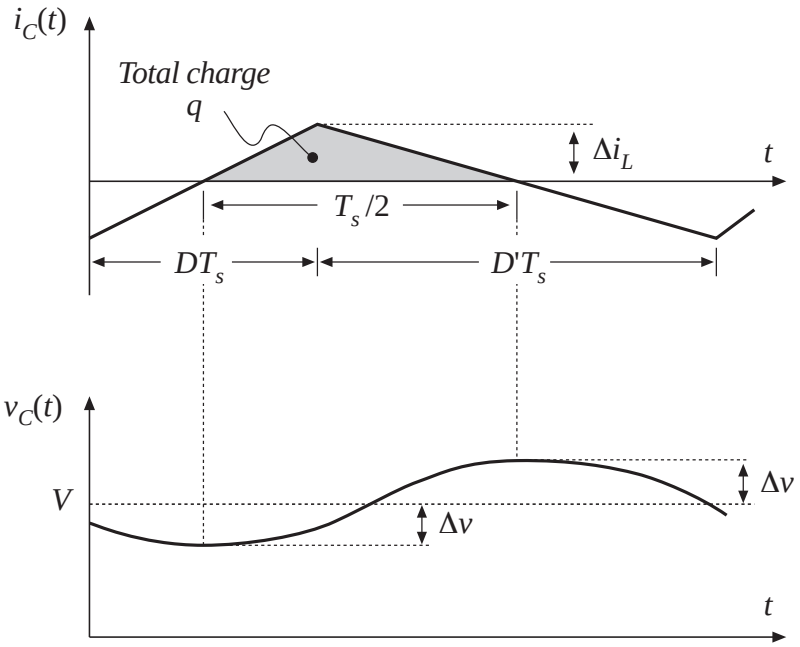
What is the capacitor current?



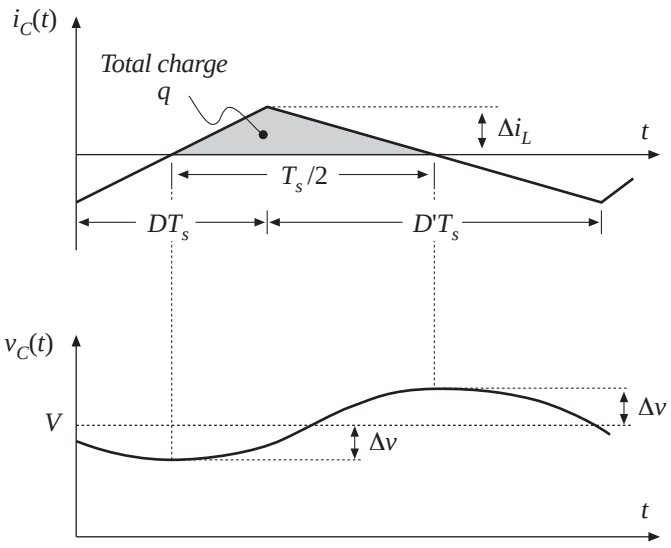
Capacitor current and voltage, buck example

Must not neglect inductor current ripple!

If the capacitor voltage ripple is small, then essentially all of the ac component of inductor current flows through the capacitor.



Estimating capacitor voltage ripple Δv

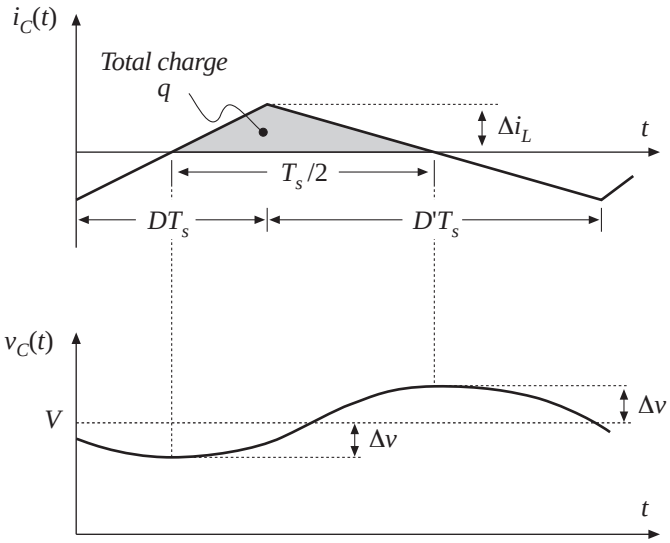


Current $i_C(t)$ is positive for half of the switching period. This positive current causes the capacitor voltage $v_C(t)$ to increase between its minimum and maximum extrema. During this time, the total charge q is deposited on the capacitor plates, where

$$q = C\,(2\Delta v)$$

(*change in charge*) = C (*change in voltage*)

Estimating capacitor voltage ripple Δv



The total charge q is the area of the triangle, as shown:

$$q = \tfrac{1}{2}\Delta i_L \frac{T_s}{2}$$

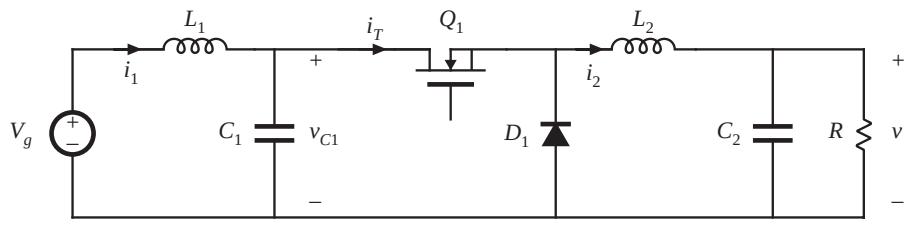
Eliminate q and solve for Δv:

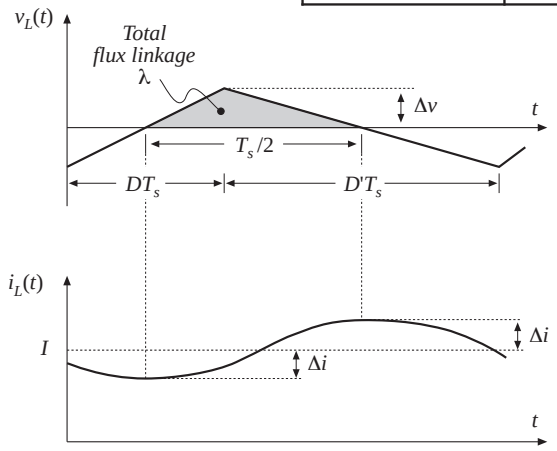
$$\Delta v = \frac{\Delta i_L \, T_s}{8 \, C}$$

Note: in practice, capacitor equivalent series resistance (esr) further increases Δv.

Inductor current ripple in two-pole filters

Example: problem 2.9





can use similar arguments, with

$$\lambda = L\,(2\Delta i)$$

λ = inductor flux linkages

= inductor volt-seconds

2.6 Summary of Key Points

1. The dc component of a converter waveform is given by its average value, or the integral over one switching period, divided by the switching period. Solution of a dc-dc converter to find its dc, or steady-state, voltages and currents therefore involves averaging the waveforms.
2. The linear ripple approximation greatly simplifies the analysis. In a well-designed converter, the switching ripples in the inductor currents and capacitor voltages are small compared to the respective dc components, and can be neglected.
3. The principle of inductor volt-second balance allows determination of the dc voltage components in any switching converter. In steady-state, the average voltage applied to an inductor must be zero.

Summary of Chapter 2

4. The principle of capacitor charge balance allows determination of the dc components of the inductor currents in a switching converter. In steady-state, the average current applied to a capacitor must be zero.
5. By knowledge of the slopes of the inductor current and capacitor voltage waveforms, the ac switching ripple magnitudes may be computed. Inductance and capacitance values can then be chosen to obtain desired ripple magnitudes.
6. In converters containing multiple-pole filters, continuous (nonpulsating) voltages and currents are applied to one or more of the inductors or capacitors. Computation of the ac switching ripple in these elements can be done using capacitor charge and/or inductor flux-linkage arguments, without use of the small-ripple approximation.
7. Converters capable of increasing (boost), decreasing (buck), and inverting the voltage polarity (buck-boost and Cuk) have been described. Converter circuits are explored more fully in a later chapter.

Chapter 3. Steady-State Equivalent Circuit Modeling, Losses, and Efficiency

3.1. The dc transformer model

3.2. Inclusion of inductor copper loss

3.3. Construction of equivalent circuit model

3.4. How to obtain the input port of the model

3.5. Example: inclusion of semiconductor conduction losses in the boost converter model

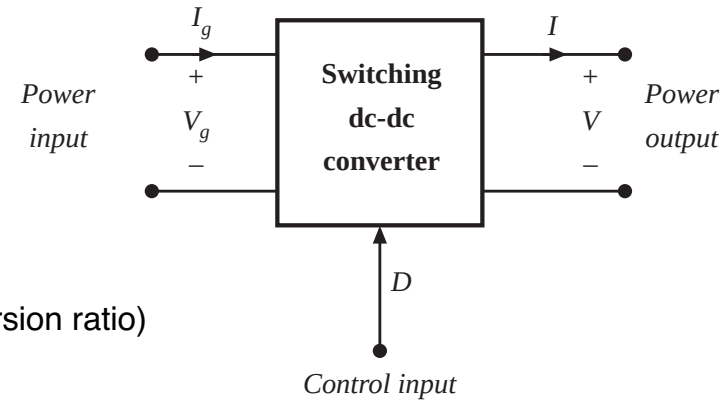
3.6. Summary of key points

3.1. The dc transformer model

Basic equations of an ideal dc-dc converter:

$P_{in} = P_{out}$

$V_g I_g = V I$ ($\eta = 100\%$)



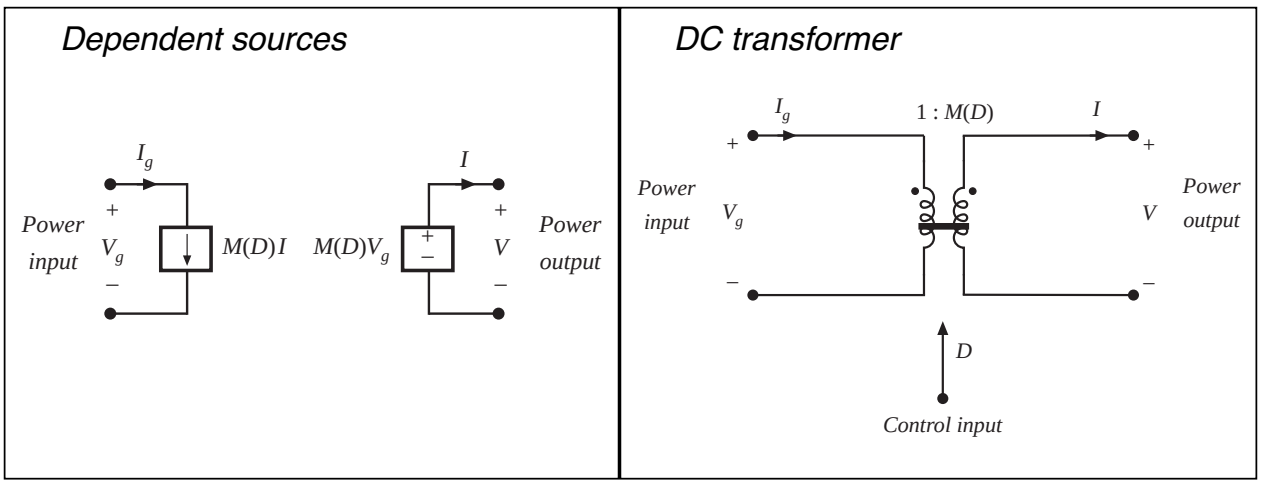
$V = M(D)\, V_g$

$I_g = M(D)\, I$ (ideal conversion ratio)

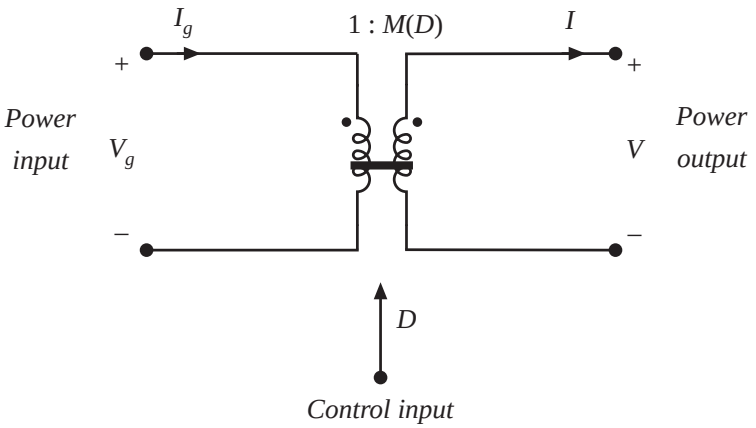
These equations are valid in steady-state. During transients, energy storage within filter elements may cause $P_{in} \neq P_{out}$

Equivalent circuits corresponding to ideal dc-dc converter equations

$$P_{in} = P_{out} \qquad V_g I_g = V I \qquad V = M(D)\, V_g \qquad I_g = M(D)\, I$$



The DC transformer model



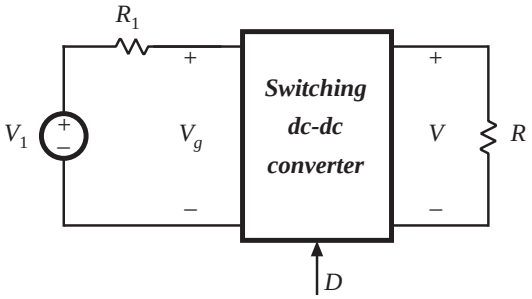
Models basic properties of ideal dc-dc converter:

- conversion of dc voltages and currents, ideally with 100% efficiency
- conversion ratio M controllable via duty cycle

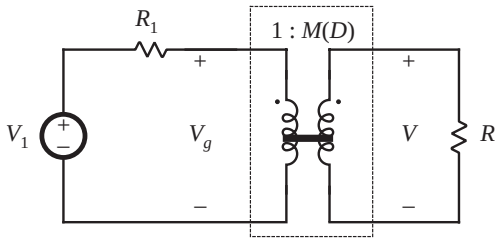
- Solid line denotes ideal transformer model, capable of passing dc voltages and currents
- Time-invariant model (no switching) which can be solved to find dc components of converter waveforms

Example: use of the DC transformer model

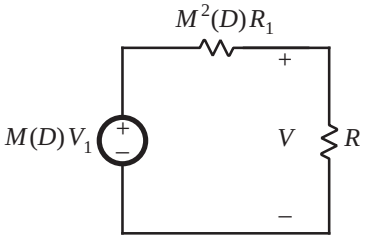
1. Original system



2. Insert dc transformer model



3. Push source through transformer



4. Solve circuit

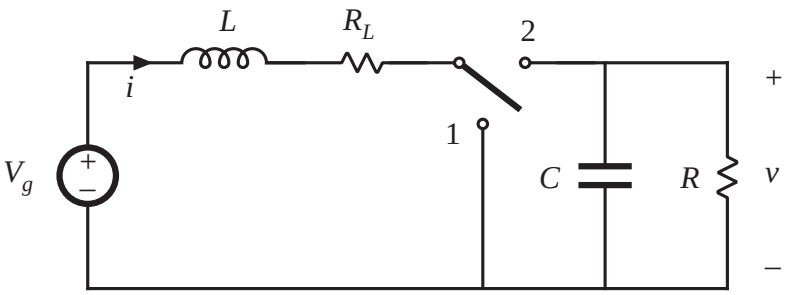
$$V = M(D)\, V_1 \, \frac{R}{R + M^2(D)\, R_1}$$

3.2. Inclusion of inductor copper loss

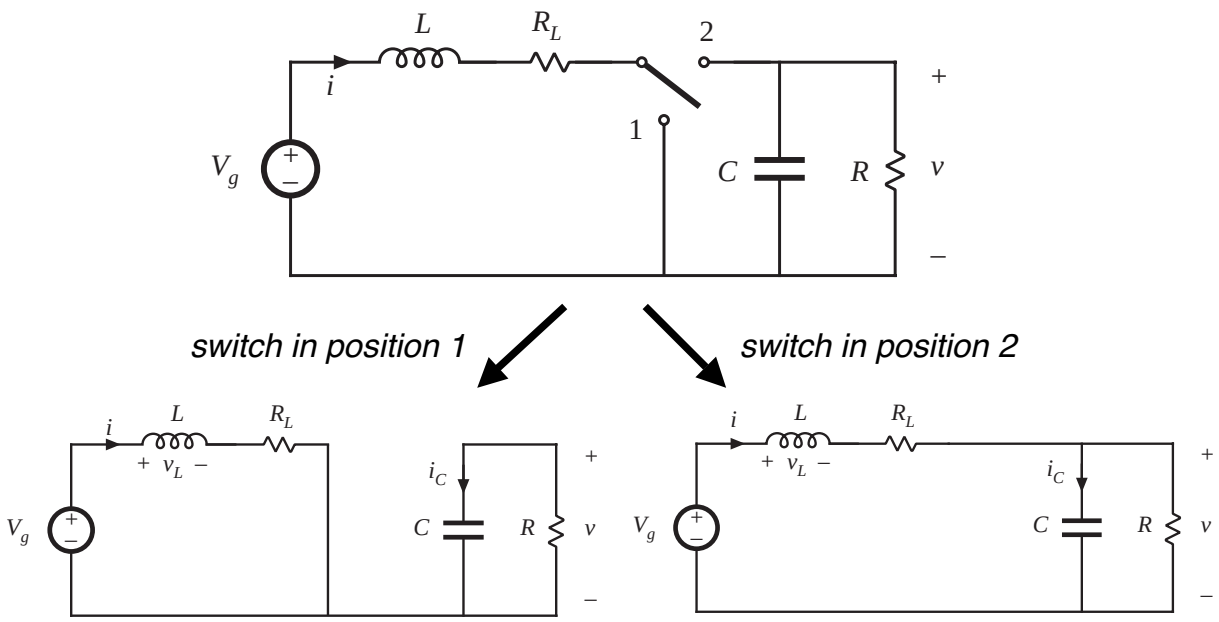
Dc transformer model can be extended, to include converter nonidealities.

Example: inductor copper loss (resistance of winding):

Insert this inductor model into boost converter circuit:



Analysis of nonideal boost converter

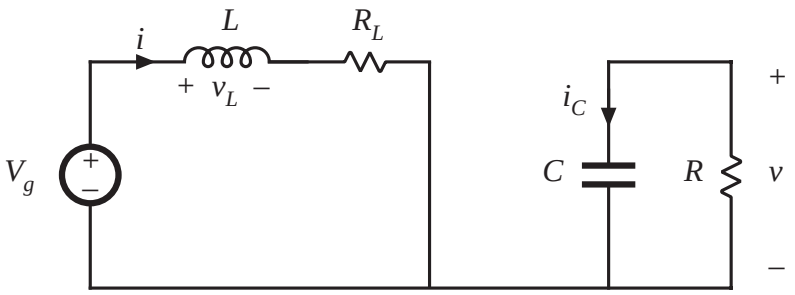


Circuit equations, switch in position 1

Inductor current and capacitor voltage:

$$v_L(t) = V_g - i(t)\, R_L$$

$$i_C(t) = -v(t) / R$$

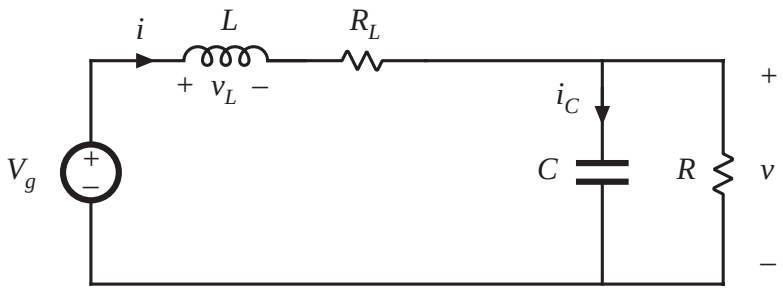


Small ripple approximation:

$$v_L(t) = V_g - I\, R_L$$

$$i_C(t) = -V / R$$

Circuit equations, switch in position 2



$$v_L(t) = V_g - i(t)\,R_L - v(t) \approx V_g - I\,R_L - V$$
$$i_C(t) = i(t) - v(t)\,/\,R \approx I - V\,/\,R$$

Inductor voltage and capacitor current waveforms

Average inductor voltage:

$$\left\langle v_L(t) \right\rangle = \frac{1}{T_s}\int_0^{T_s} v_L(t)dt$$
$$= D(V_g - I\,R_L) + D'(V_g - I\,R_L - V)$$

Inductor volt-second balance:

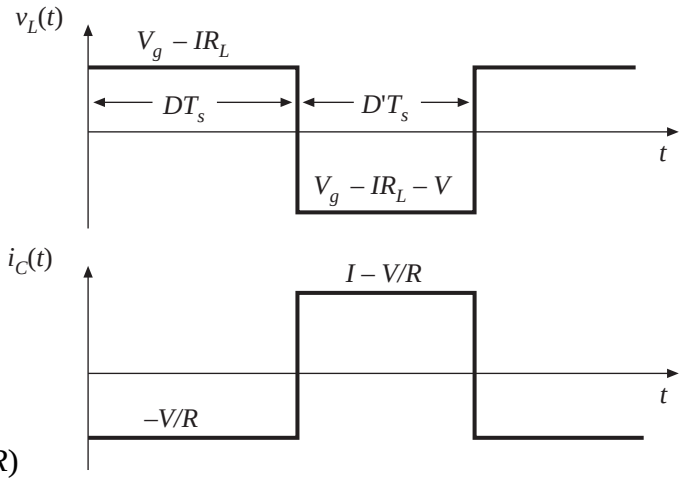
$$0 = V_g - I\,R_L - D'V$$

Average capacitor current:

$$\left\langle i_C(t) \right\rangle = D\,(-V\,/\,R) + D'\,(I - V\,/\,R)$$

Capacitor charge balance:

$$0 = D'I - V\,/\,R$$



Solution for output voltage

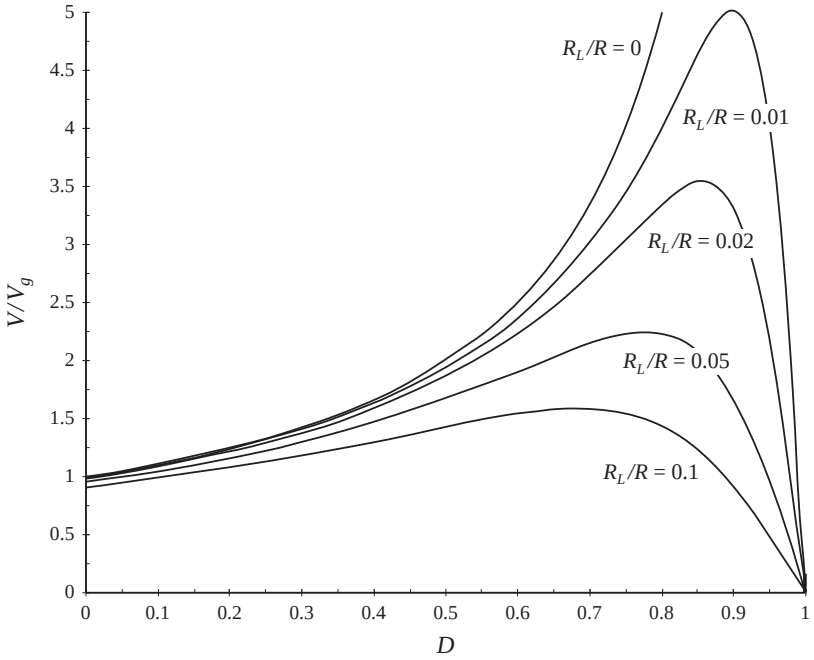
We now have two equations and two unknowns:

$$0 = V_g - I\,R_L - D'V$$

$$0 = D'I - V / R$$

Eliminate I and solve for V:

$$\frac{V}{V_g} = \frac{1}{D'}\,\frac{1}{(1 + R_L / D'^2 R)}$$



3.3. Construction of equivalent circuit model

Results of previous section (derived via inductor volt-sec balance and capacitor charge balance):

$$\langle v_L \rangle = 0 = V_g - I\,R_L - D'V$$

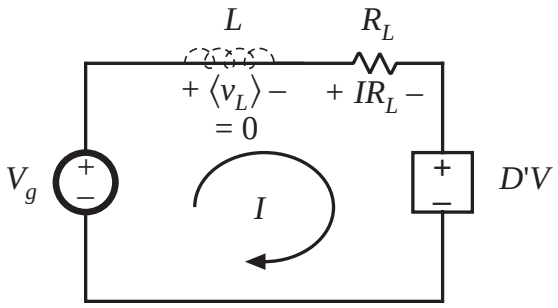
$$\langle i_C \rangle = 0 = D'I - V / R$$

View these as loop and node equations of the equivalent circuit. Reconstruct an equivalent circuit satisfying these equations

Inductor voltage equation

$$\langle v_L \rangle = 0 = V_g - I\,R_L - D'V$$

- Derived via Kirchhoff's voltage law, to find the inductor voltage during each subinterval
- Average inductor voltage then set to zero
- This is a loop equation: the dc components of voltage around a loop containing the inductor sum to zero

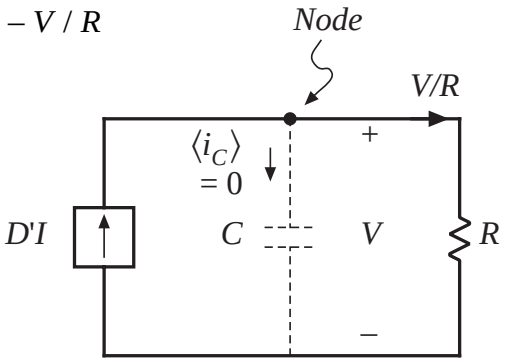


- IR_L term: voltage across resistor of value R_L having current I
- $D'V$ term: for now, leave as dependent source

Capacitor current equation

$$\langle i_C \rangle = 0 = D'I - V / R$$

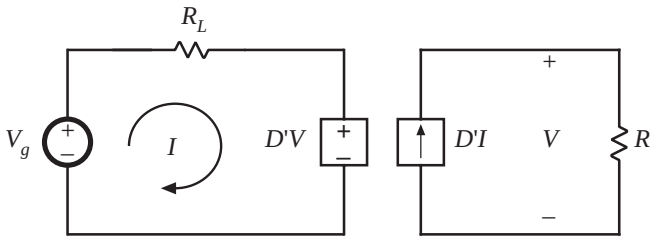
- Derived via Kirchoff's current law, to find the capacitor current during each subinterval
- Average capacitor current then set to zero
- This is a node equation: the dc components of current flowing into a node connected to the capacitor sum to zero



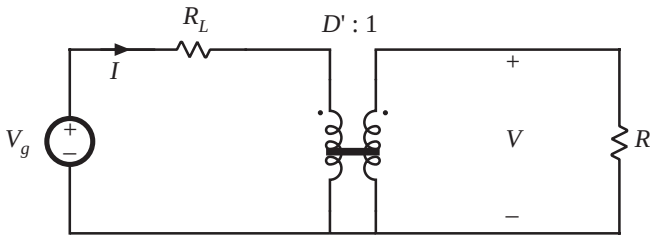
- V/R term: current through load resistor of value R having voltage V
- $D'I$ term: for now, leave as dependent source

Complete equivalent circuit

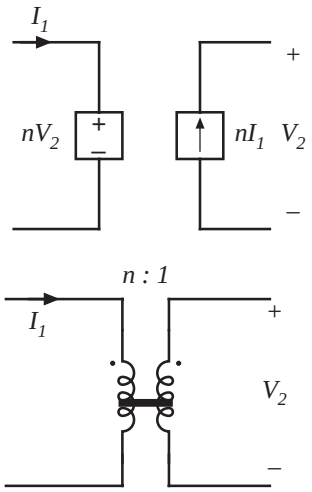
The two circuits, drawn together:



The dependent sources are equivalent to a $D' : 1$ transformer:



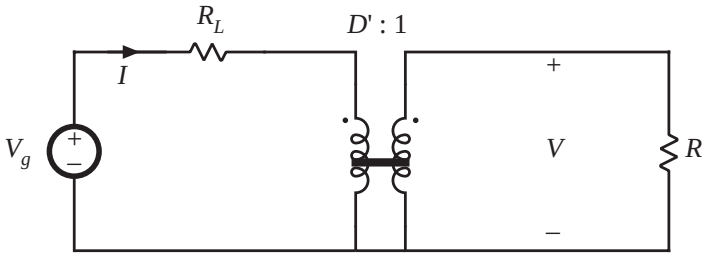
Dependent sources and transformers



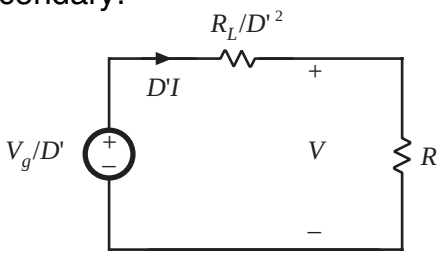
- *sources have same coefficient*
- *reciprocal voltage/current dependence*

Solution of equivalent circuit

Converter equivalent circuit



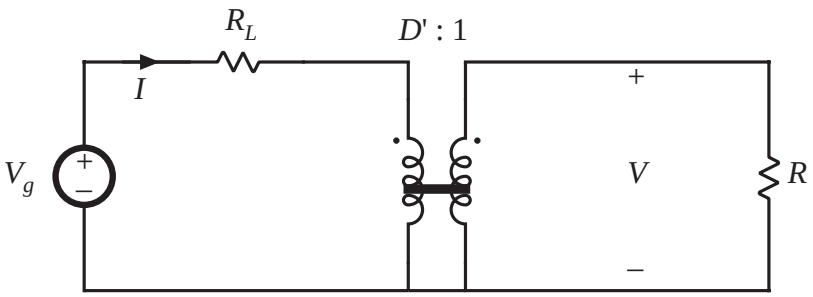
Refer all elements to transformer secondary:



Solution for output voltage using voltage divider formula:

$$V = \frac{V_g}{D'} \frac{R}{R + \frac{R_L}{D'^2}} = \frac{V_g}{D'} \frac{1}{1 + \frac{R_L}{D'^2 R}}$$

Solution for input (inductor) current

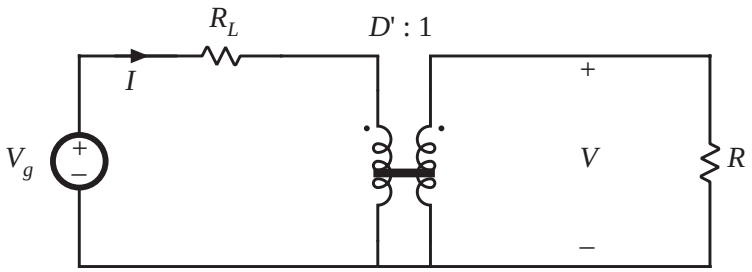


$$I = \frac{V_g}{D'^2 R + R_L} = \frac{V_g}{D'^2} \frac{1}{1 + \frac{R_L}{D'^2 R}}$$

Solution for converter efficiency

$$P_{in} = (V_g)\,(I)$$

$$P_{out} = (V)\,(D'I)$$

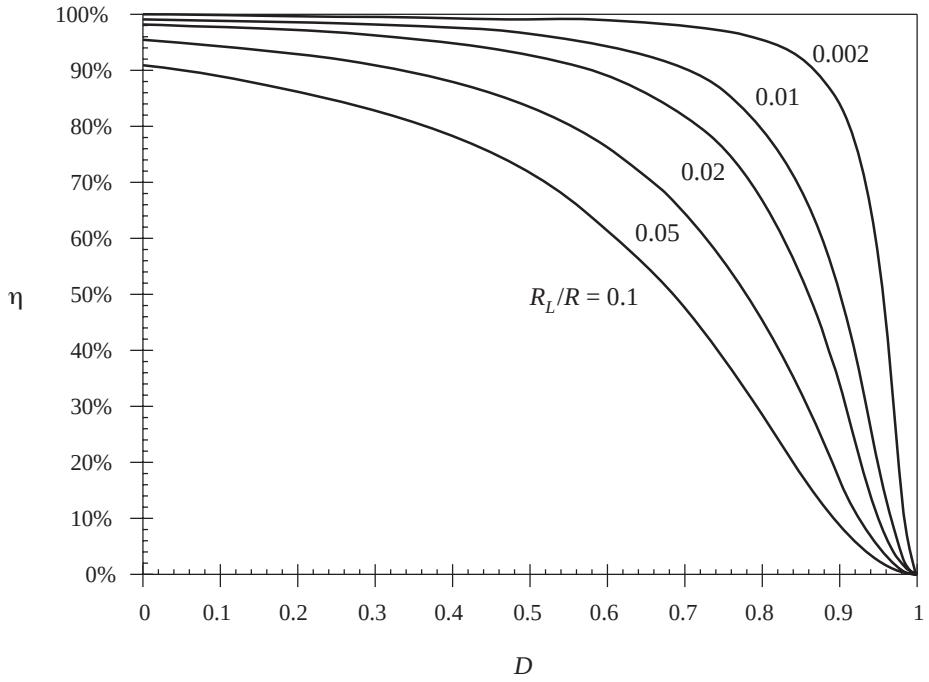


$$\eta = \frac{P_{out}}{P_{in}} = \frac{(V)\,(D'I)}{(V_g)\,(I)} = \frac{V}{V_g} D'$$

$$\eta = \frac{1}{1 + \frac{R_L}{D'^2 R}}$$

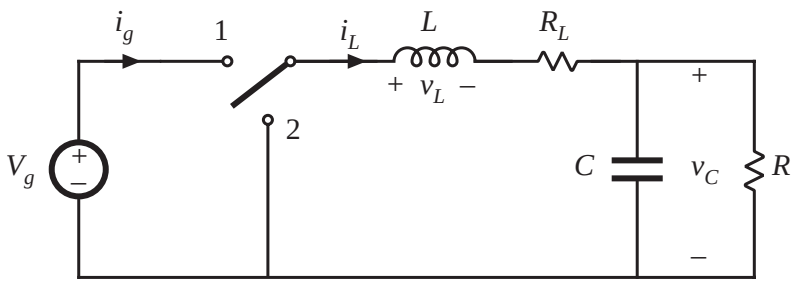
Efficiency, for various values of R_L

$$\eta = \frac{1}{1 + \frac{R_L}{D'^2 R}}$$



3.4. How to obtain the input port of the model

Buck converter example —use procedure of previous section to derive equivalent circuit

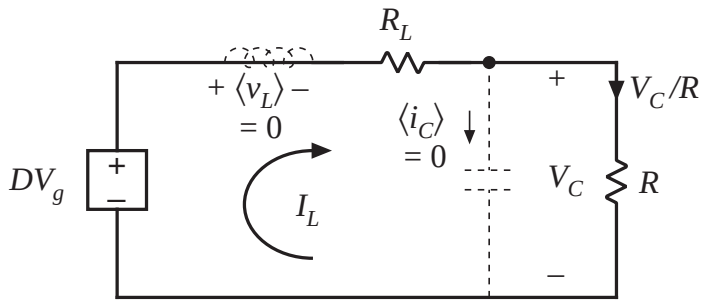


Average inductor voltage and capacitor current:

$$\langle v_L \rangle = 0 = DV_g - I_L R_L - V_C \qquad \langle i_C \rangle = 0 = I_L - V_C/R$$

Construct equivalent circuit as usual

$$\langle v_L \rangle = 0 = DV_g - I_L R_L - V_C \qquad \langle i_C \rangle = 0 = I_L - V_C/R$$

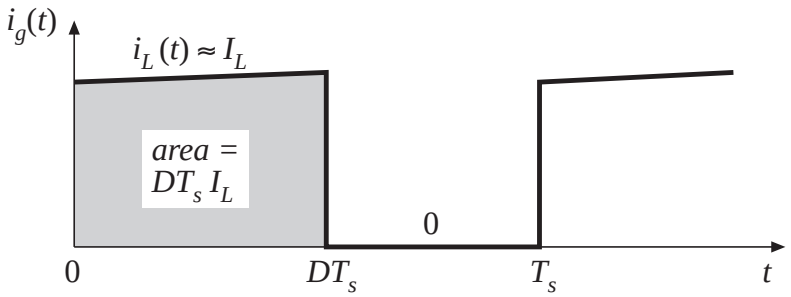


What happened to the transformer?

- Need another equation

Modeling the converter input port

Input current waveform $i_g(t)$:

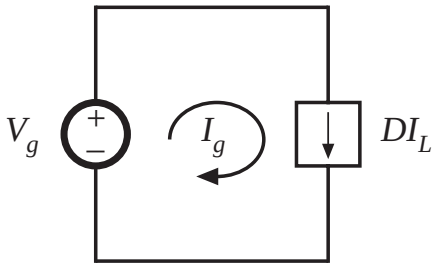


Dc component (average value) of $i_g(t)$ is

$$I_g = \frac{1}{T_s} \int_0^{T_s} i_g(t)\, dt = DI_L$$

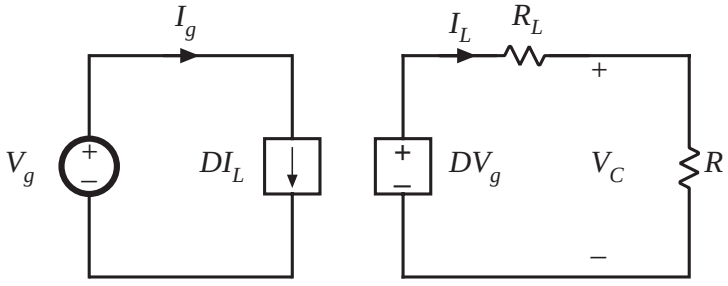
Input port equivalent circuit

$$I_g = \frac{1}{T_s}\int_0^{T_s} i_g(t)\,dt = DI_L$$

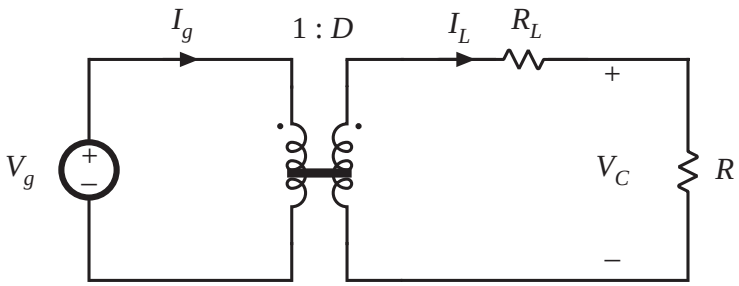


Complete equivalent circuit, buck converter

Input and output port equivalent circuits, drawn together:

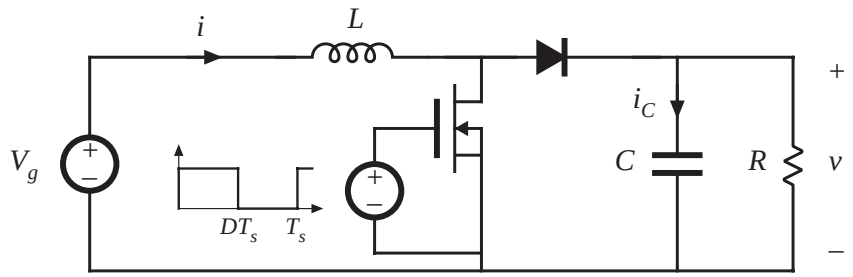


Replace dependent sources with equivalent dc transformer:



3.5. Example: inclusion of semiconductor conduction losses in the boost converter model

Boost converter example



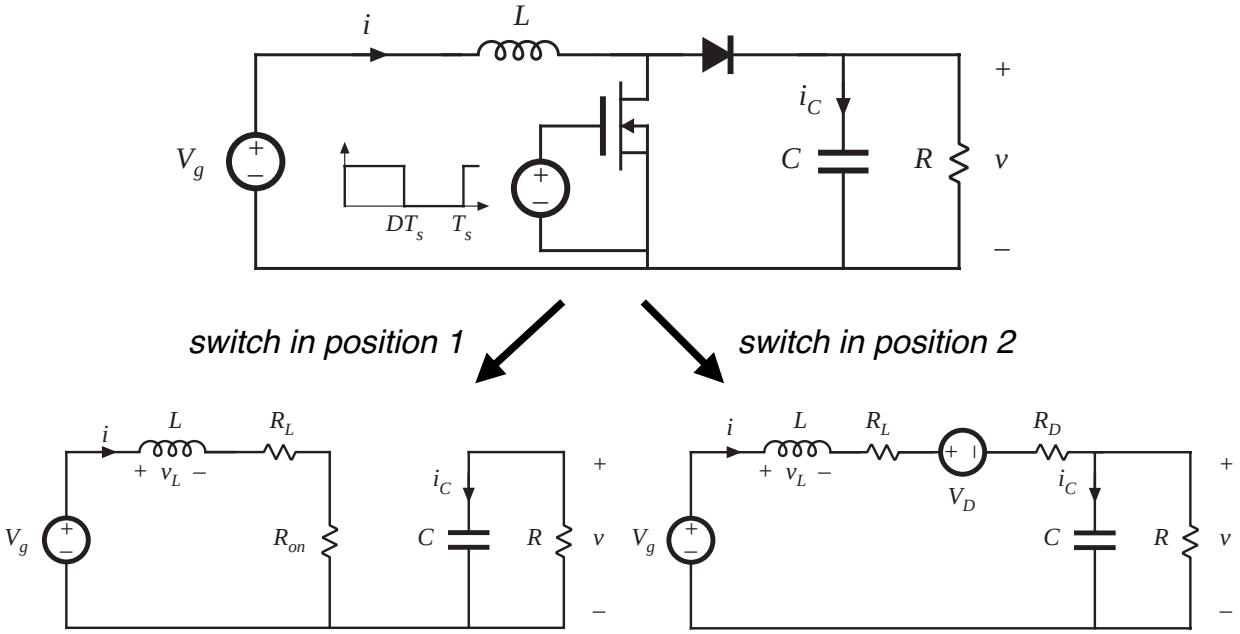
Models of on-state semiconductor devices:

MOSFET: on-resistance R_{on}

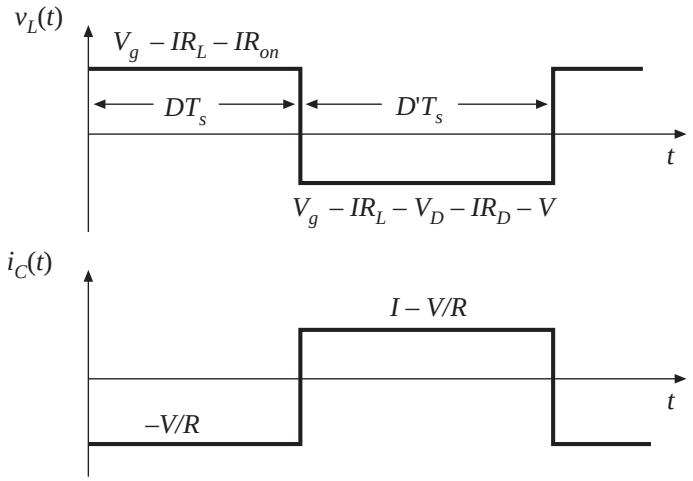
Diode: constant forward voltage V_D plus on-resistance R_D

Insert these models into subinterval circuits

Boost converter example: circuits during subintervals 1 and 2



Average inductor voltage and capacitor current

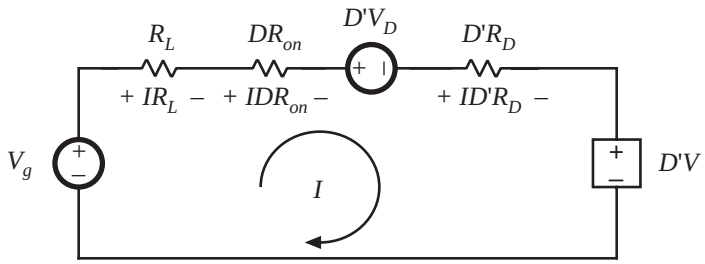


$$\langle v_L \rangle = D(V_g - IR_L - IR_{on}) + D'(V_g - IR_L - V_D - IR_D - V) = 0$$

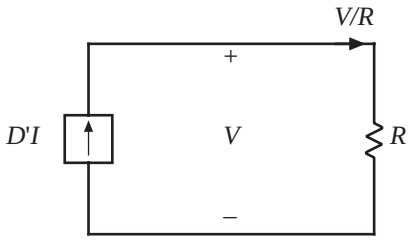
$$\langle i_C \rangle = D(-V/R) + D'(I - V/R) = 0$$

Construction of equivalent circuits

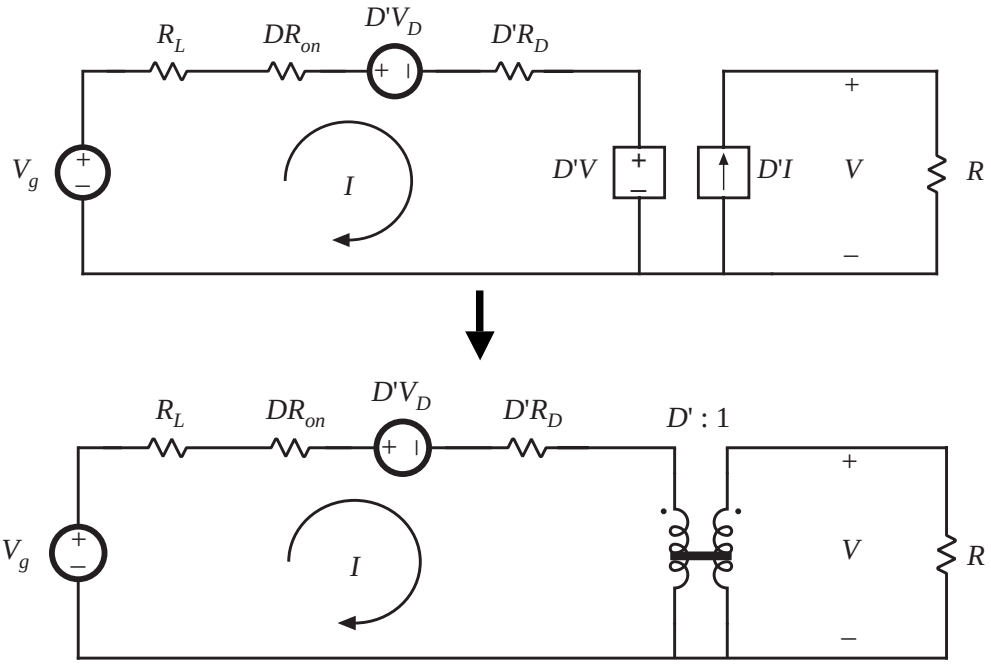
$$V_g - IR_L - IDR_{on} - D'V_D - ID'R_D - D'V = 0$$



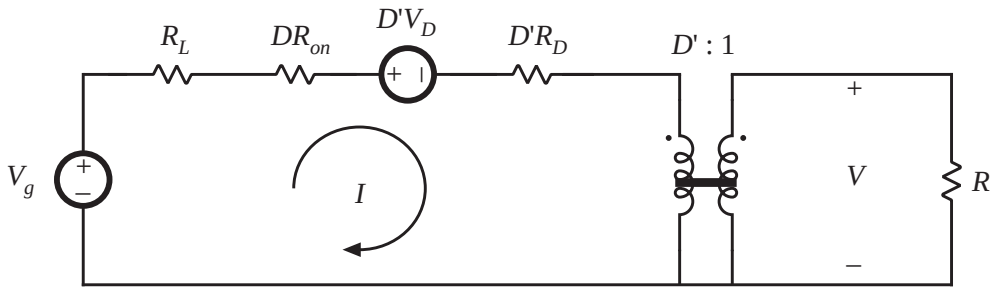
$$D'I - V/R = 0$$



Complete equivalent circuit



Solution for output voltage



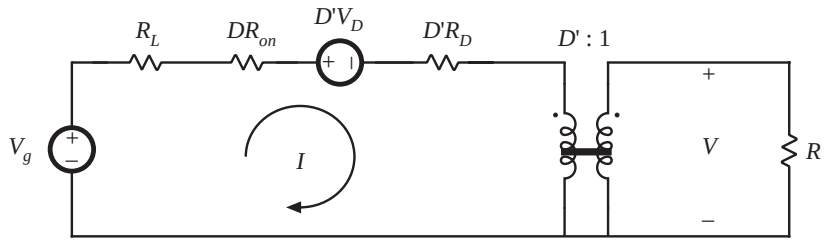
$$V = \left(\frac{1}{D'}\right)\left(V_g - D'V_D\right)\left(\frac{D'^2R}{D'^2R + R_L + DR_{on} + D'R_D}\right)$$

$$\frac{V}{V_g} = \left(\frac{1}{D'}\right)\left(1 - \frac{D'V_D}{V_g}\right)\left(\frac{1}{1 + \dfrac{R_L + DR_{on} + D'R_D}{D'^2R}}\right)$$

Solution for converter efficiency

$$P_{in} = (V_g)\,(I)$$

$$P_{out} = (V)\,(D'I)$$



$$\eta = D'\,\frac{V}{V_g} = \frac{\left(1 - \dfrac{D'V_D}{V_g}\right)}{\left(1 + \dfrac{R_L + DR_{on} + D'R_D}{D'^2 R}\right)}$$

Conditions for high efficiency:

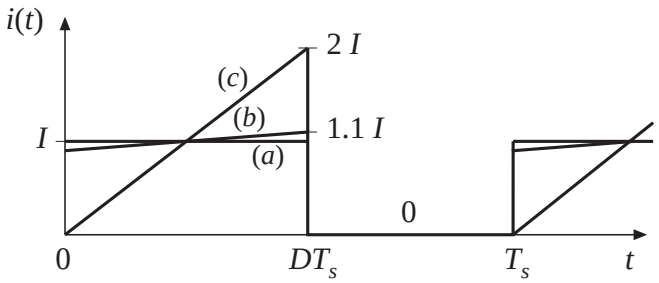
$$V_g/D' \gg V_D$$

$$D'^2 R \gg R_L + DR_{on} + D'R_D$$

Accuracy of the averaged equivalent circuit in prediction of losses

- Model uses average currents and voltages
- To correctly predict power loss in a resistor, use rms values
- Result is the same, provided ripple is small

MOSFET current waveforms, for various ripple magnitudes:



Inductor current ripple	*MOSFET rms current*	*Average power loss in R_{on}*
(a) $\Delta i = 0$	$I\sqrt{D}$	$D\,I^2\,R_{on}$
(b) $\Delta i = 0.1\,I$	$(1.00167)\,I\sqrt{D}$	$(1.0033)\,D\,I^2\,R_{on}$
(c) $\Delta i = I$	$(1.155)\,I\sqrt{D}$	$(1.3333)\,D\,I^2\,R_{on}$

Summary of chapter 3

1. The dc transformer model represents the primary functions of any dc-dc converter: transformation of dc voltage and current levels, ideally with 100% efficiency, and control of the conversion ratio M via the duty cycle D. This model can be easily manipulated and solved using familiar techniques of conventional circuit analysis.
2. The model can be refined to account for loss elements such as inductor winding resistance and semiconductor on-resistances and forward voltage drops. The refined model predicts the voltages, currents, and efficiency of practical nonideal converters.
3. In general, the dc equivalent circuit for a converter can be derived from the inductor volt-second balance and capacitor charge balance equations. Equivalent circuits are constructed whose loop and node equations coincide with the volt-second and charge balance equations. In converters having a pulsating input current, an additional equation is needed to model the converter input port; this equation may be obtained by averaging the converter input current.

Chapter 4. Switch Realization

4.1. Switch applications

Single-, two-, and four-quadrant switches. Synchronous rectifiers

4.2. A brief survey of power semiconductor devices

Power diodes, MOSFETs, BJTs, IGBTs, and thyristors

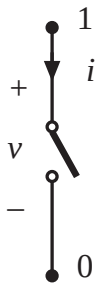
4.3. Switching loss

Transistor switching with clamped inductive load. Diode recovered charge. Stray capacitances and inductances, and ringing. Efficiency vs. switching frequency.

4.4. Summary of key points

SPST (single-pole single-throw) switches

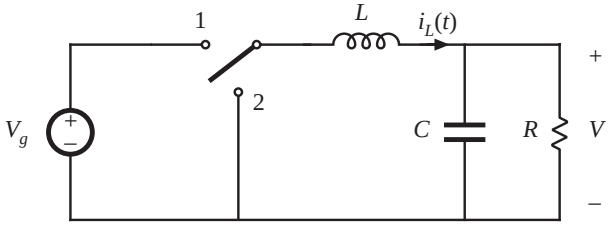
SPST switch, with voltage and current polarities defined



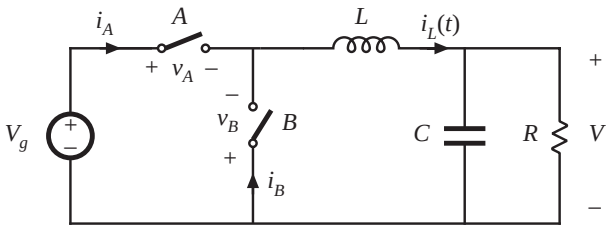
All power semiconductor devices function as SPST switches.

Buck converter

with SPDT switch:



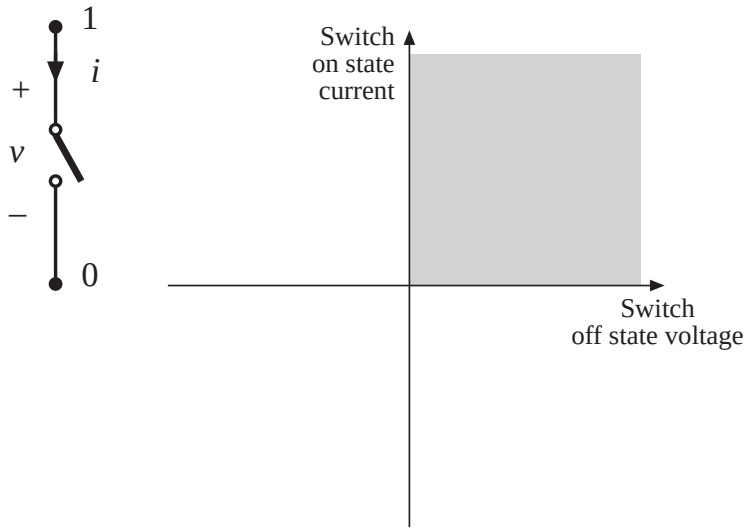
with two SPST switches:



Realization of SPDT switch using two SPST switches

- A nontrivial step: two SPST switches are not exactly equivalent to one SPDT switch
- It is possible for both SPST switches to be simultaneously ON or OFF
- Behavior of converter is then significantly modified —discontinuous conduction modes (chapter 5)
- Conducting state of SPST switch may depend on applied voltage or current —for example: diode

Quadrants of SPST switch operation



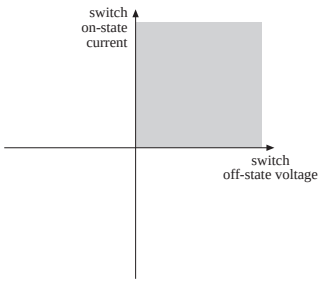
A single-quadrant switch example:

ON-state: $i > 0$

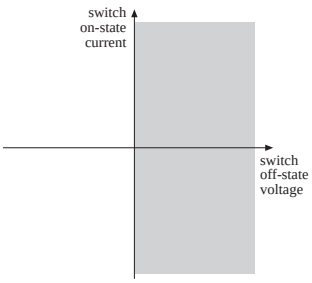
OFF-state: $v > 0$

Some basic switch applications

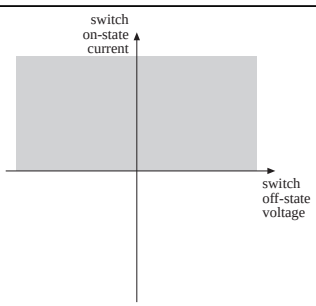
Single-quadrant switch



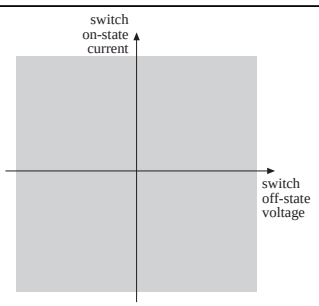
Current-bidirectional two-quadrant switch



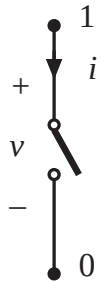
Voltage-bidirectional two-quadrant switch



Four-quadrant switch



4.1.1. Single-quadrant switches



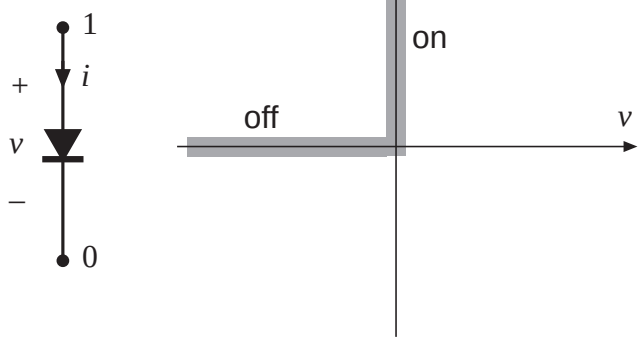
Active switch: Switch state is controlled exclusively by a third terminal (control terminal).

Passive switch: Switch state is controlled by the applied current and/or voltage at terminals 1 and 2.

SCR: A special case — turn-on transition is active, while turn-off transition is passive.

Single-quadrant switch: on-state $i(t)$ and off-state $v(t)$ are unipolar.

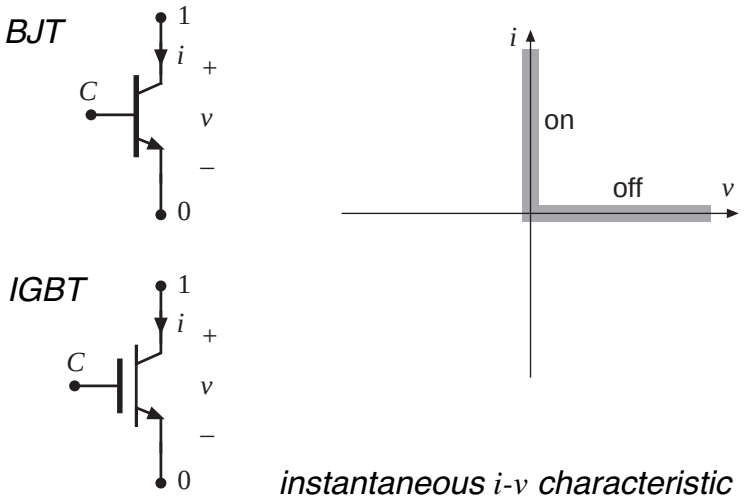
The diode



Symbol *instantaneous i-v characteristic*

- *A passive switch*
- *Single-quadrant switch:*
- *can conduct positive on-state current*
- *can block negative off-state voltage*
- *provided that the intended on-state and off-state operating points lie on the diode i-v characteristic, then switch can be realized using a diode*

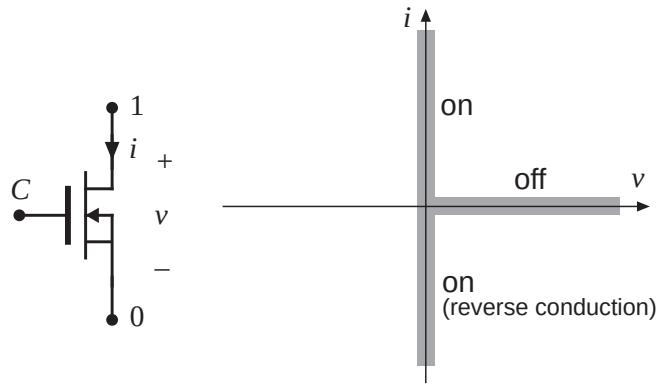
The Bipolar Junction Transistor (BJT) and the Insulated Gate Bipolar Transistor (IGBT)



instantaneous i-v characteristic

- *An active switch, controlled by terminal C*
- *Single-quadrant switch:*
- *can conduct positive on-state current*
- *can block positive off-state voltage*
- *provided that the intended on-state and off-state operating points lie on the transistor i-v characteristic, then switch can be realized using a BJT or IGBT*

The Metal-Oxide Semiconductor Field Effect Transistor (MOSFET)

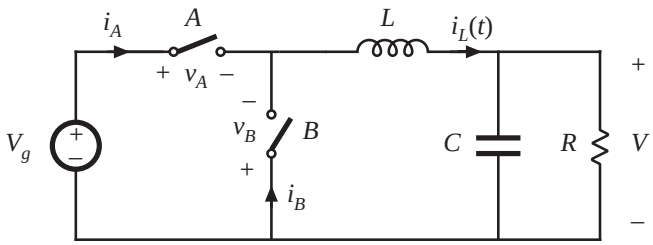


Symbol *instantaneous i-v characteristic*

- *An active switch, controlled by terminal C*
- *Normally operated as single-quadrant switch:*
- *can conduct positive on-state current (can also conduct negative current in some circumstances)*
- *can block positive off-state voltage*
- *provided that the intended on-state and off-state operating points lie on the MOSFET i-v characteristic, then switch can be realized using a MOSFET*

Realization of switch using transistors and diodes

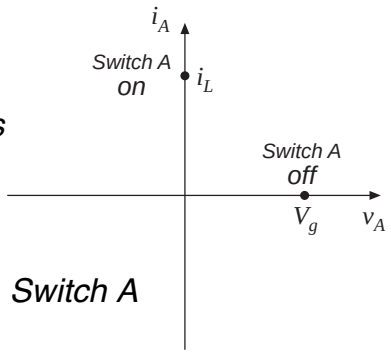
Buck converter example



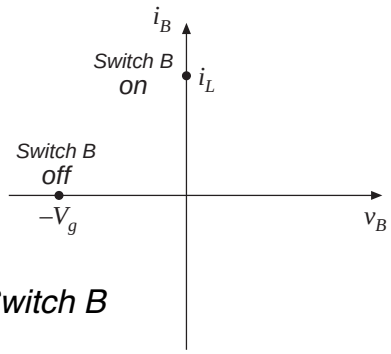
Switch A: transistor

Switch B: diode

SPST switch operating points

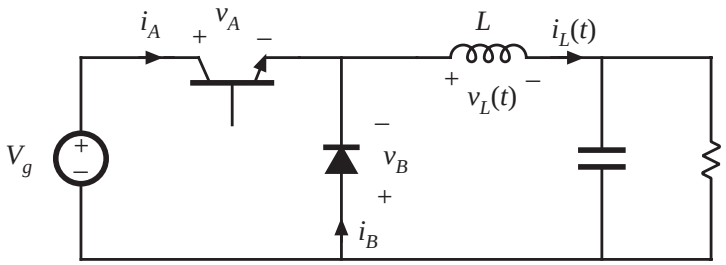


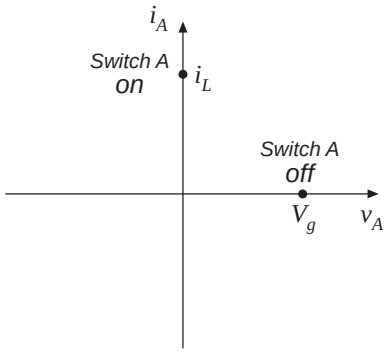
Switch A

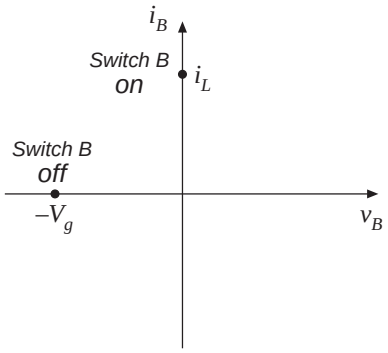


Switch B

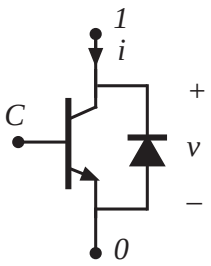
Realization of buck converter using single-quadrant switches



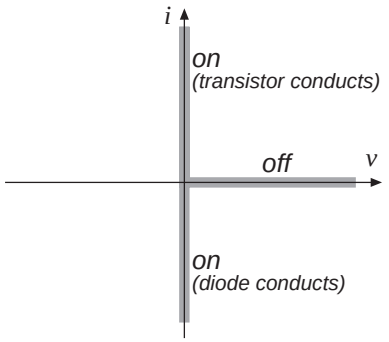




4.1.2. Current-bidirectional two-quadrant switches



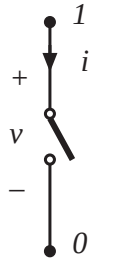
BJT / anti-parallel diode realization

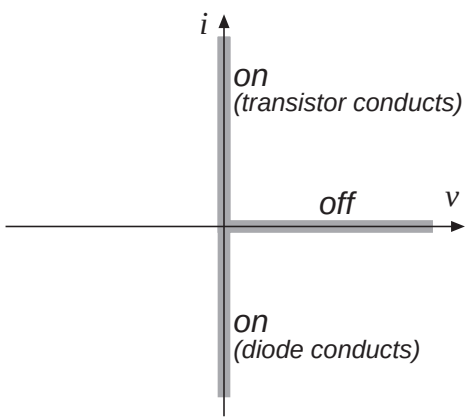


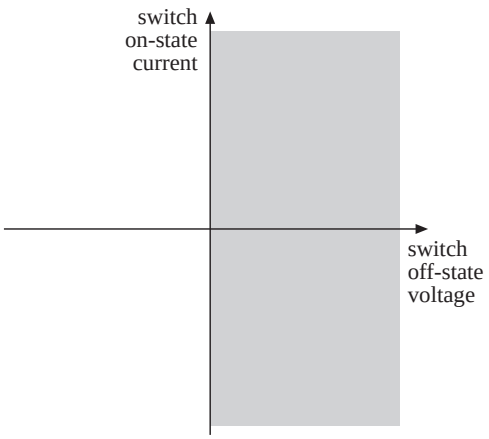
instantaneous i-v characteristic

- *Usually an active switch, controlled by terminal C*
- *Normally operated as two-quadrant switch:*
- *can conduct positive or negative on-state current*
- *can block positive off-state voltage*
- *provided that the intended on-state and off-state operating points lie on the composite i-v characteristic, then switch can be realized as shown*

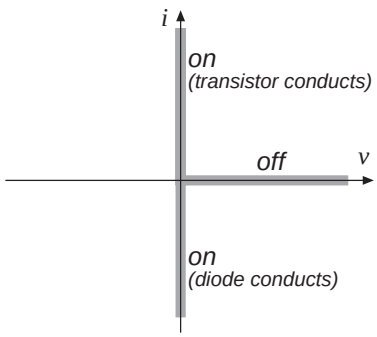
Two quadrant switches



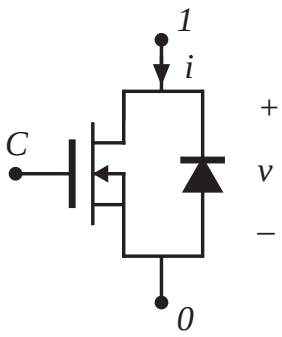




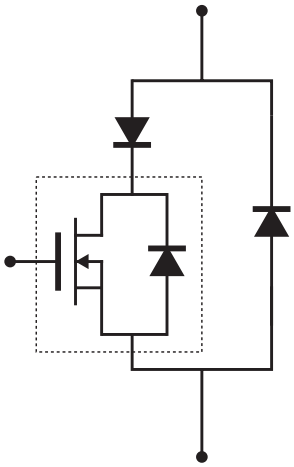
MOSFET body diode



Power MOSFET characteristics

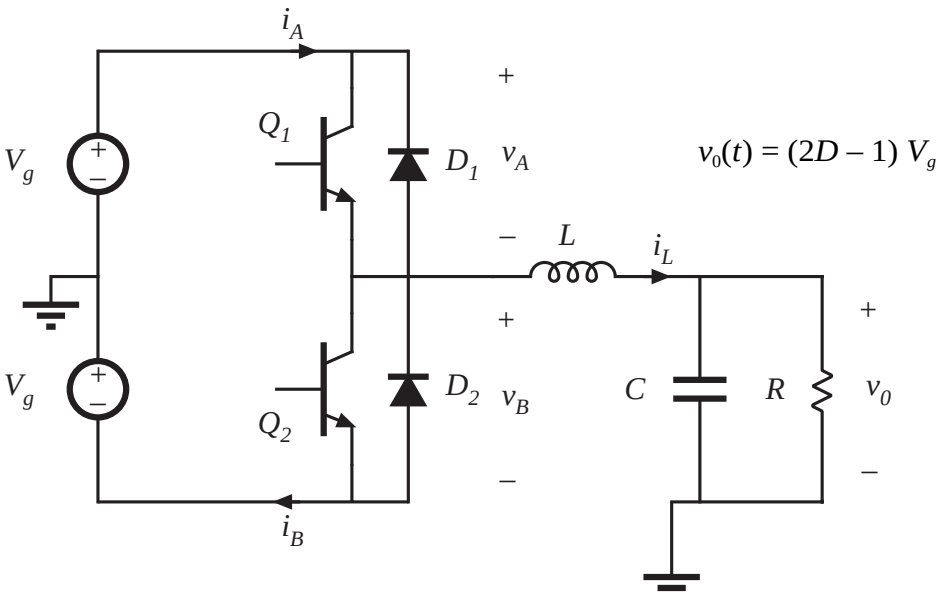


Power MOSFET, and its integral body diode



Use of external diodes to prevent conduction of body diode

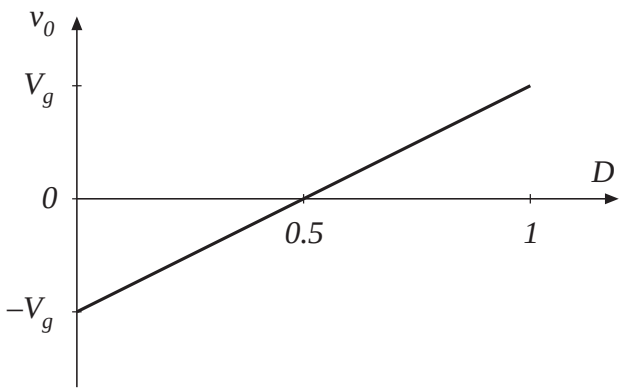
A simple inverter



$v_0(t) = (2D - 1)\, V_g$

Inverter: sinusoidal modulation of D

$$v_0(t) = (2D - 1)\, V_g$$



Sinusoidal modulation to produce ac output:

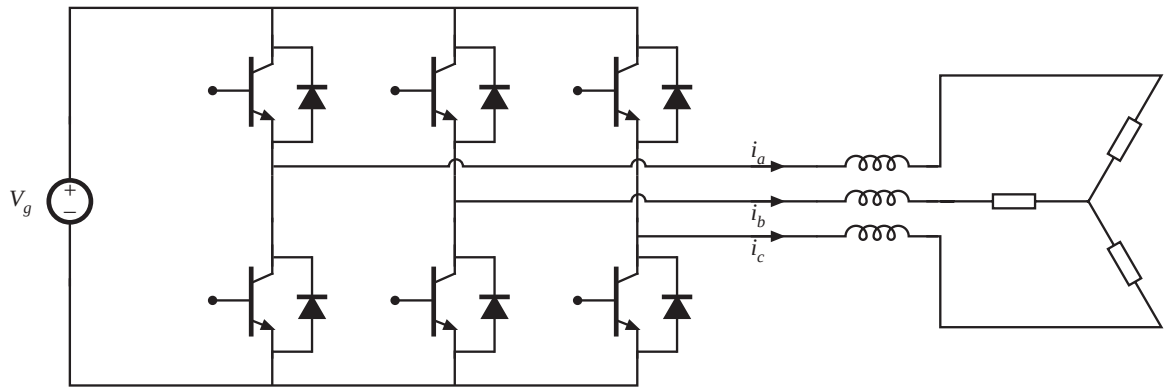
$$D(t) = 0.5 + D_m \sin(\omega t)$$

The resulting inductor current variation is also sinusoidal:

$$i_L(t) = \frac{v_0(t)}{R} = (2D - 1)\, \frac{V_g}{R}$$

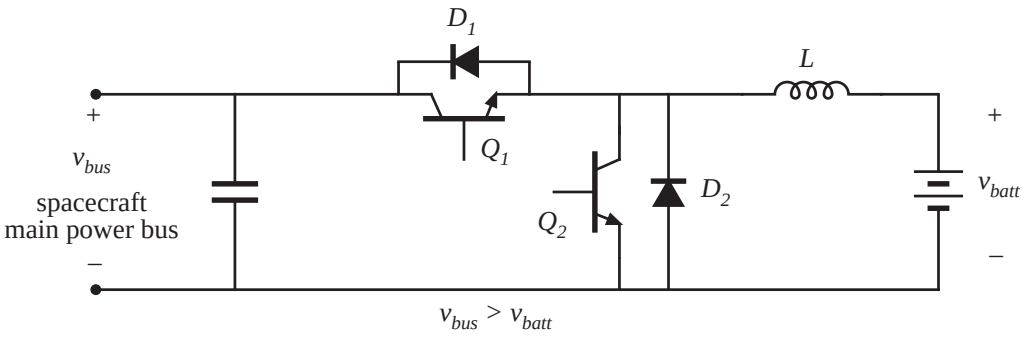
Hence, current-bidirectional two-quadrant switches are required.

The dc-3øac voltage source inverter (VSI)



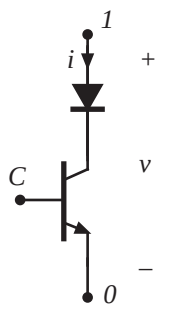
Switches must block dc input voltage, and conduct ac load current.

Bidirectional battery charger/discharger

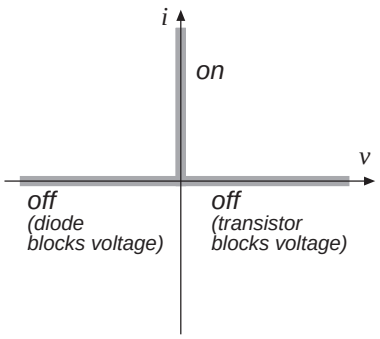


A dc-dc converter with bidirectional power flow.

4.1.3. Voltage-bidirectional two-quadrant switches



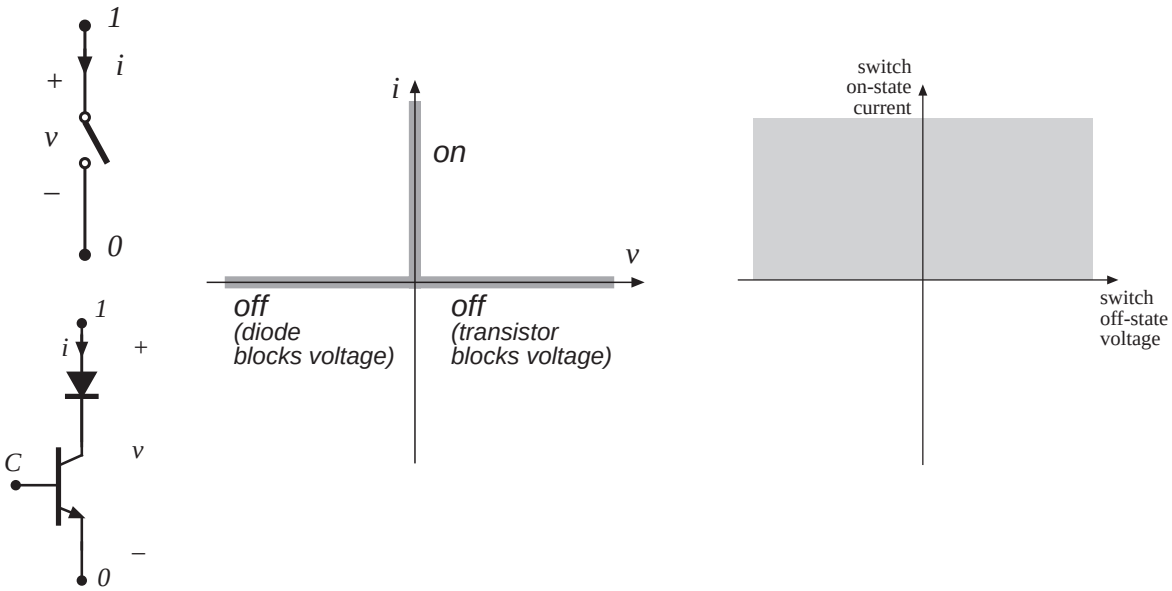
BJT / series diode realization



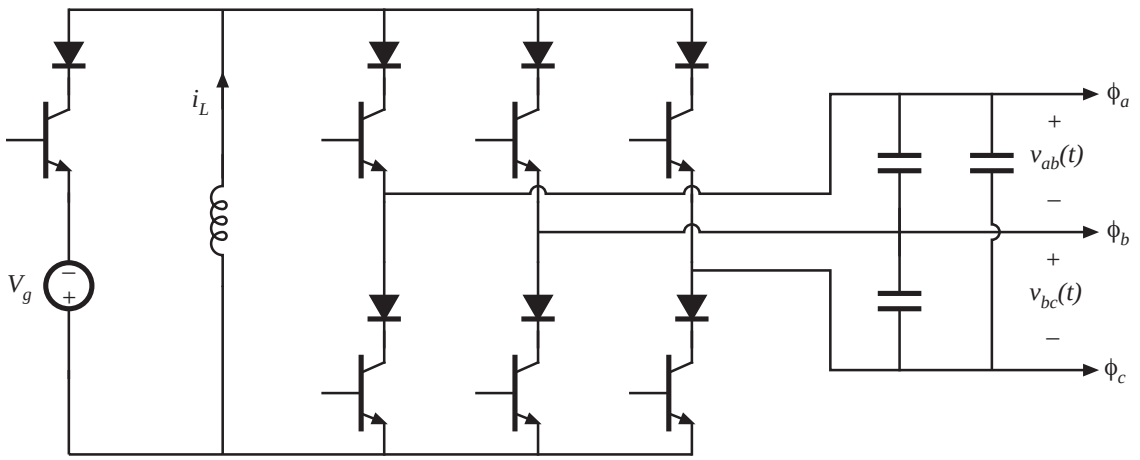
instantaneous i-v characteristic

- *Usually an active switch, controlled by terminal C*
- *Normally operated as two-quadrant switch:*
- *can conduct positive on-state current*
- *can block positive or negative off-state voltage*
- *provided that the intended on-state and off-state operating points lie on the composite i-v characteristic, then switch can be realized as shown*
- *The SCR is such a device, without controlled turn-off*

Two-quadrant switches



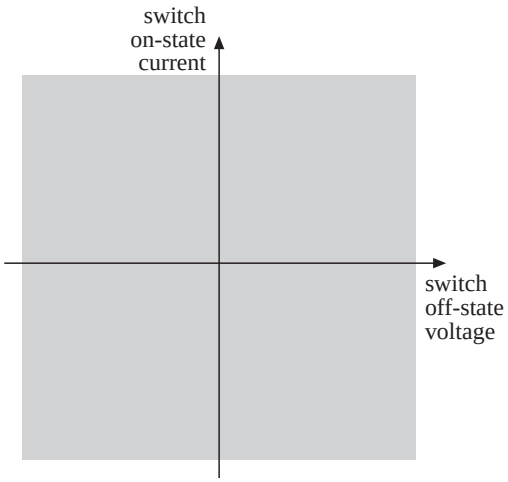
A dc-3øac buck-boost inverter



Requires voltage-bidirectional two-quadrant switches.

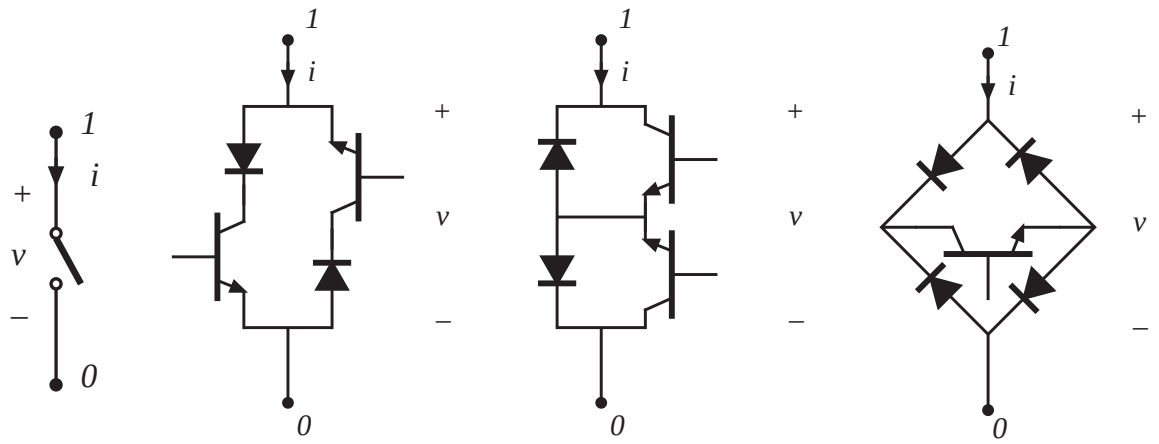
Another example: boost-type inverter, or current-source inverter (CSI).

4.1.4. Four-quadrant switches

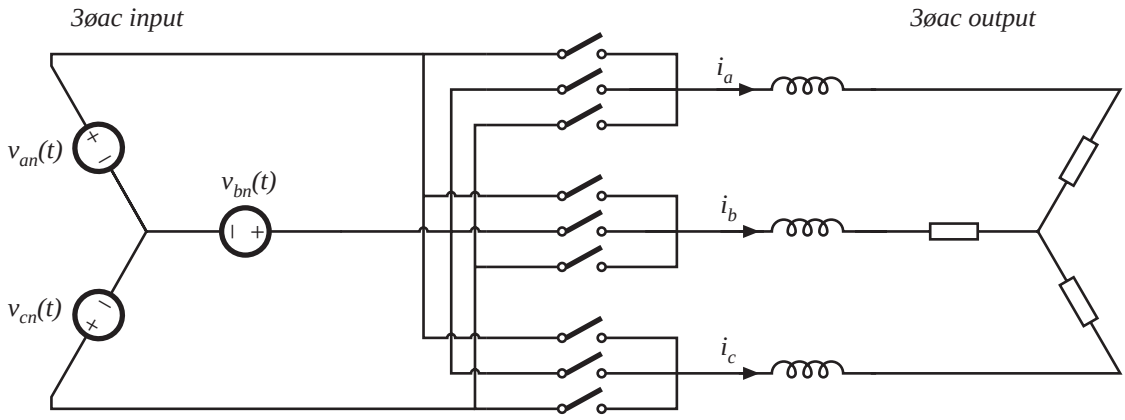


- *Usually an active switch, controlled by terminal C*
- *can conduct positive or negative on-state current*
- *can block positive or negative off-state voltage*

Three ways to realize a four-quadrant switch



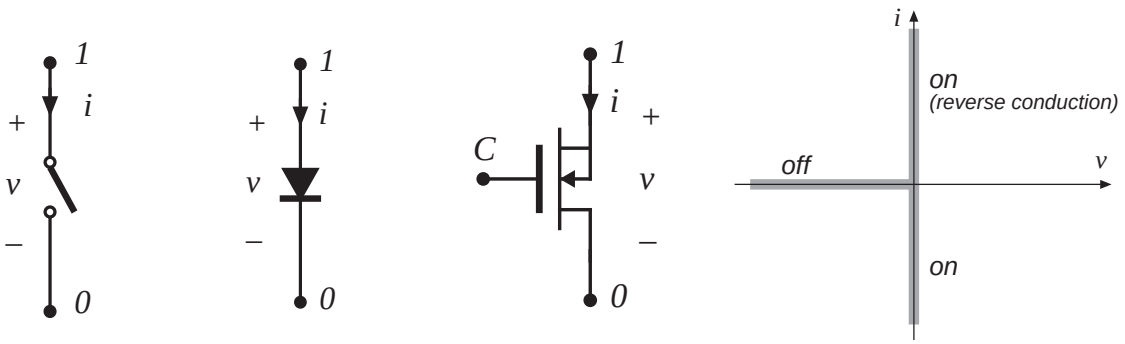
A 3øac-3øac matrix converter



- All voltages and currents are ac; hence, four-quadrant switches are required.
- Requires nine four-quadrant switches

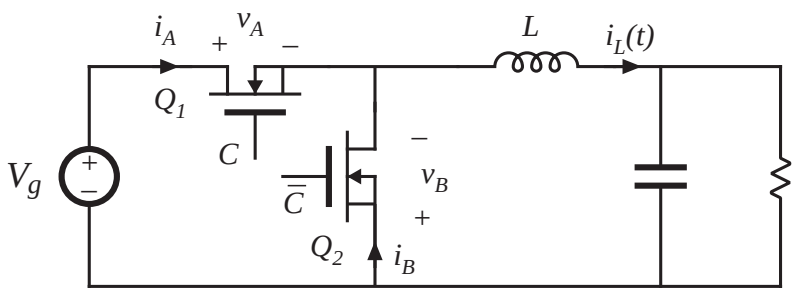
4.1.5. Synchronous rectifiers

Replacement of diode with a backwards-connected MOSFET,
to obtain reduced conduction loss



ideal switch *conventional diode rectifier* *MOSFET as synchronous rectifier* *instantaneous i-v characteristic*

Buck converter with synchronous rectifier



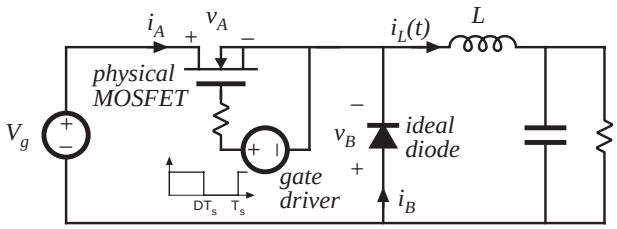
- MOSFET Q_2 is controlled to turn on when diode would normally conduct
- Semiconductor conduction loss can be made arbitrarily small, by reduction of MOSFET on-resistances
- Useful in low-voltage high-current applications

4.2. A brief survey of power semiconductor devices

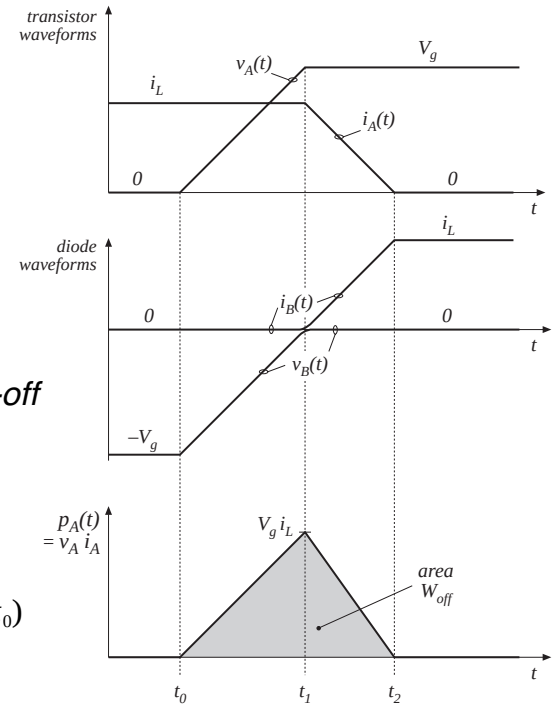
- Power diodes
- Power MOSFETs
- Bipolar Junction Transistors (BJTs)
- Insulated Gate Bipolar Transistors (IGBTs)
- Thyristors (SCR, GTO, MCT)

- On resistance vs. breakdown voltage vs. switching times
- Minority carrier and majority carrier devices

4.3.1. Transistor switching with clamped inductive load



Buck converter example



$v_B(t) = v_A(t) - V_g$

$i_A(t) + i_B(t) = i_L$

transistor turn-off transition

$$W_{off} = \tfrac{1}{2}\, V_g i_L\, (t_2 - t_0)$$

Switching loss induced by transistor turn-off transition

Energy lost during transistor turn-off transition:

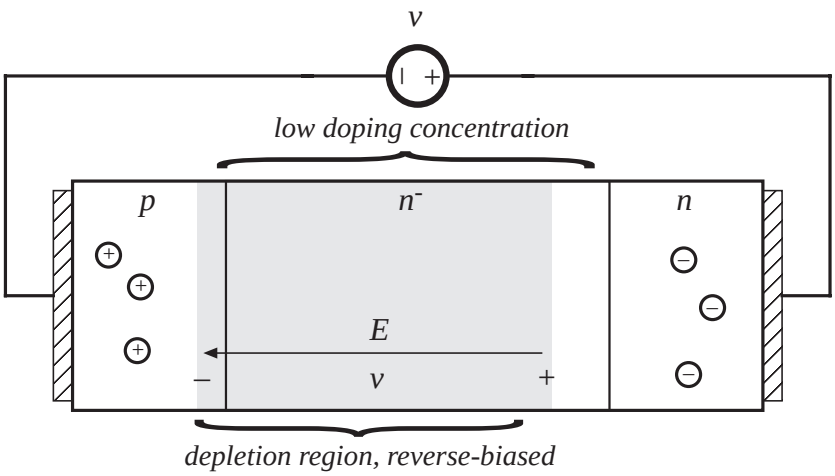
$$W_{off} = \tfrac{1}{2}\, V_g i_L\, (t_2 - t_0)$$

Similar result during transistor turn-on transition.
Average power loss:

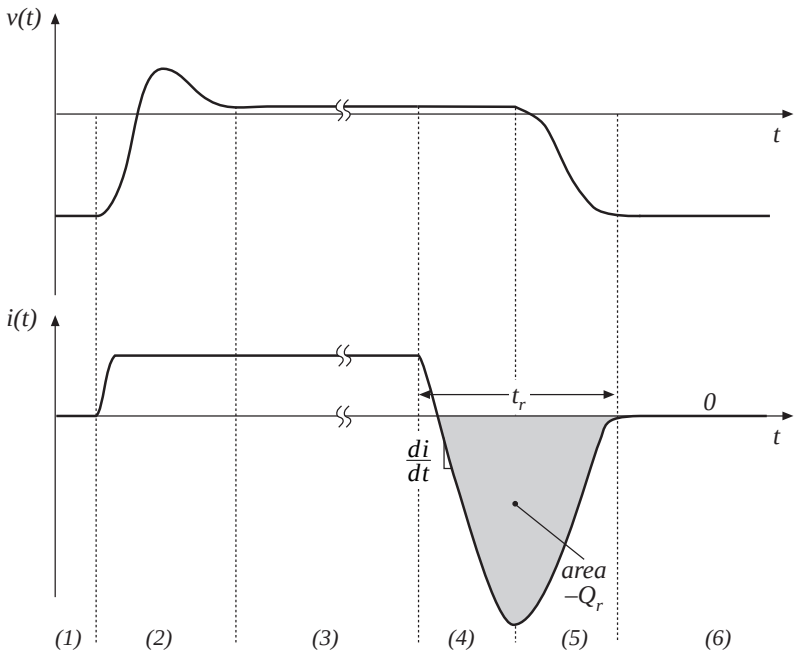
$$P_{sw} = \frac{1}{T_s} \int_{\substack{\text{switching} \\ \text{transitions}}} p_A(t)\, dt = (W_{on} + W_{off})\, f_s$$

4.2.1. Power diodes

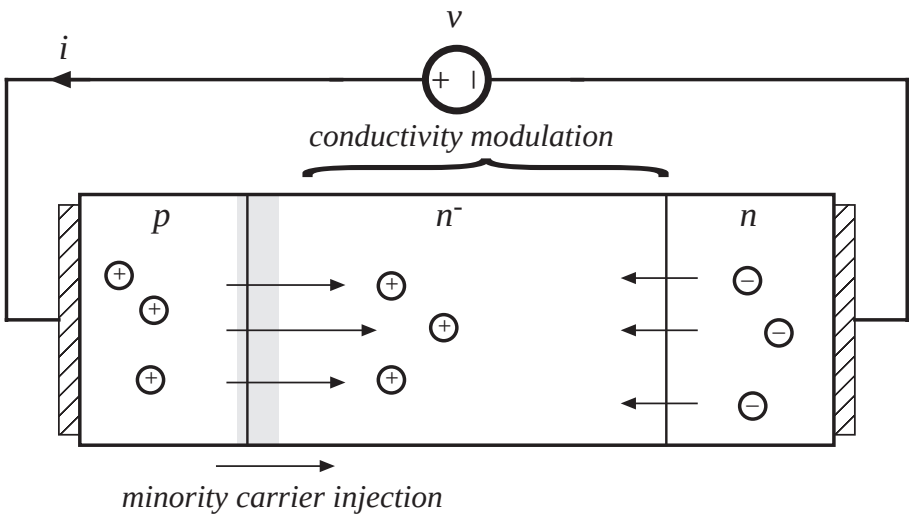
A power diode, under reverse-biased conditions:



Typical diode switching waveforms



Forward-biased power diode



Charge-controlled behavior of the diode

The diode equation:

$$q(t) = Q_0\left(e^{\lambda v(t)} - 1\right)$$

Charge control equation:

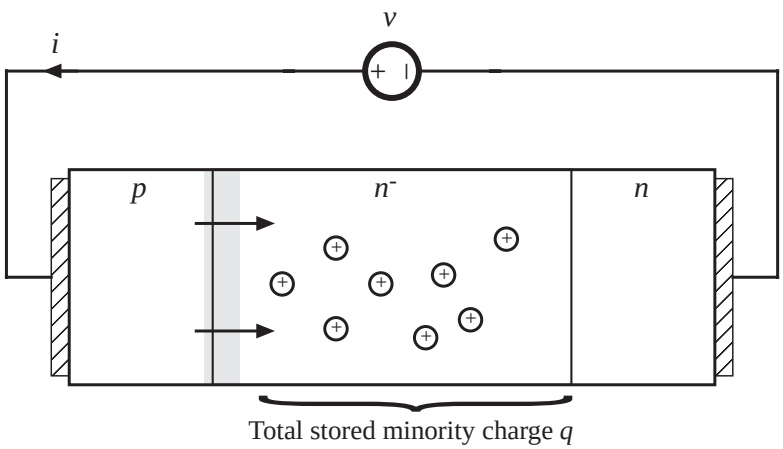
$$\frac{dq(t)}{dt} = i(t) - \frac{q(t)}{\tau_L}$$

With:

λ= 1/(26 mV) at 300 K

τ_L = minority carrier lifetime

(above equations don't include current that charges depletion region capacitance)



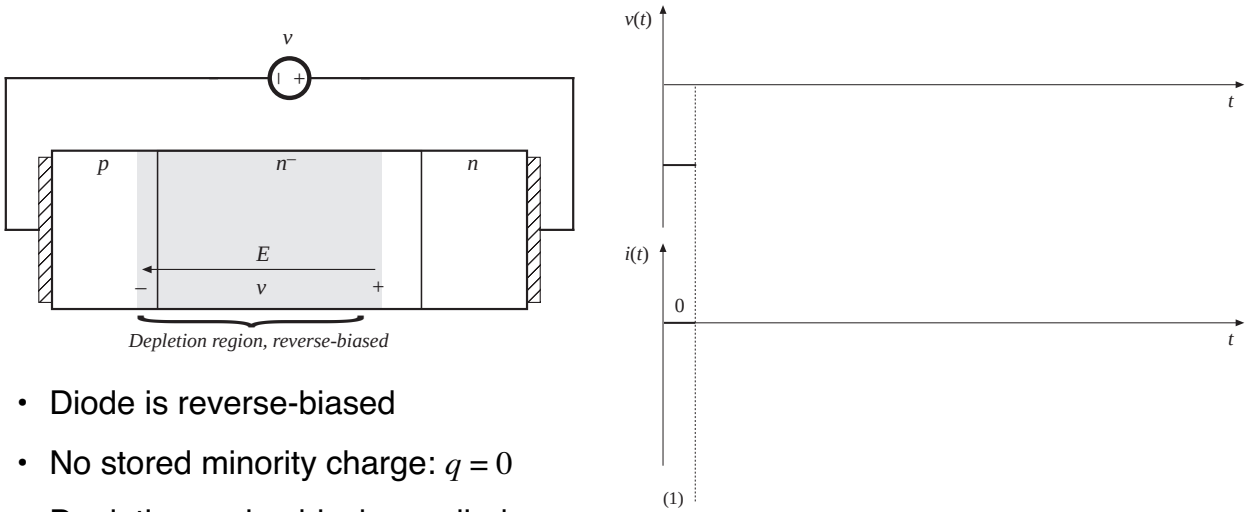
In equilibrium: $dq/dt = 0$, and hence

$$i(t) = \frac{q(t)}{\tau_L} = \frac{Q_0}{\tau_L}\left(e^{\lambda v(t)} - 1\right) = I_0\left(e^{\lambda v(t)} - 1\right)$$

Charge-control in the diode: Discussion

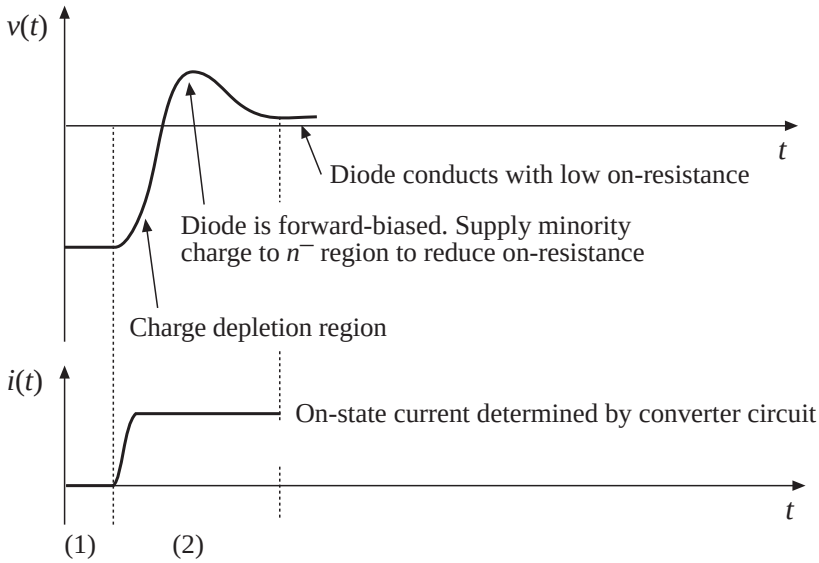
- The familiar i–v curve of the diode is an equilibrium relationship that can be violated during transient conditions
- During the turn-on and turn-off switching transients, the current deviates substantially from the equilibrium i–v curve, because of change in the stored charge and change in the charge within the reverse-bias depletion region
- Under forward-biased conditions, the stored minority charge causes “conductivity modulation” of the resistance of the lightly-doped n^- region, reducing the device on-resistance

Diode in OFF state: reversed-biased, blocking voltage



- Diode is reverse-biased
- No stored minority charge: $q = 0$
- Depletion region blocks applied reverse voltage; charge is stored in capacitance of depletion region

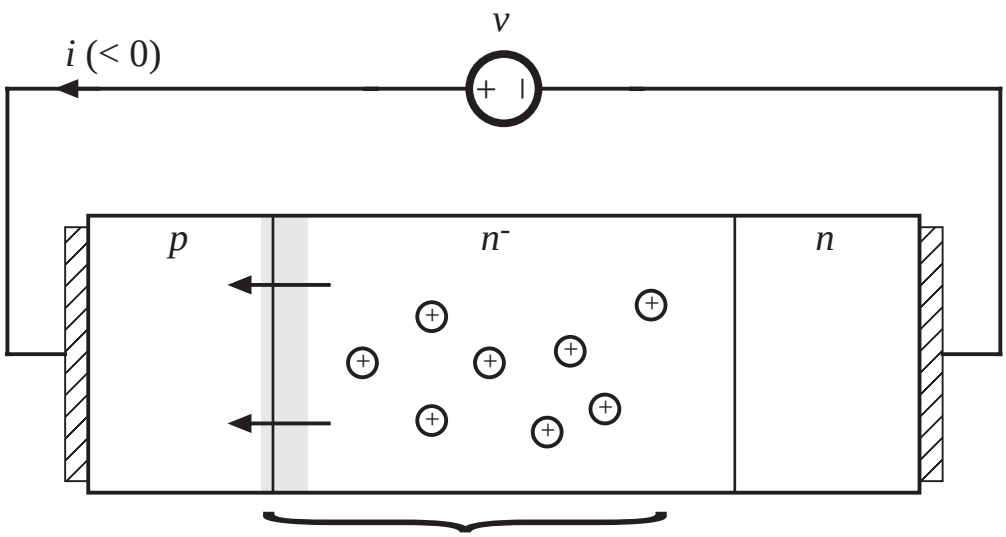
Turn-on transient



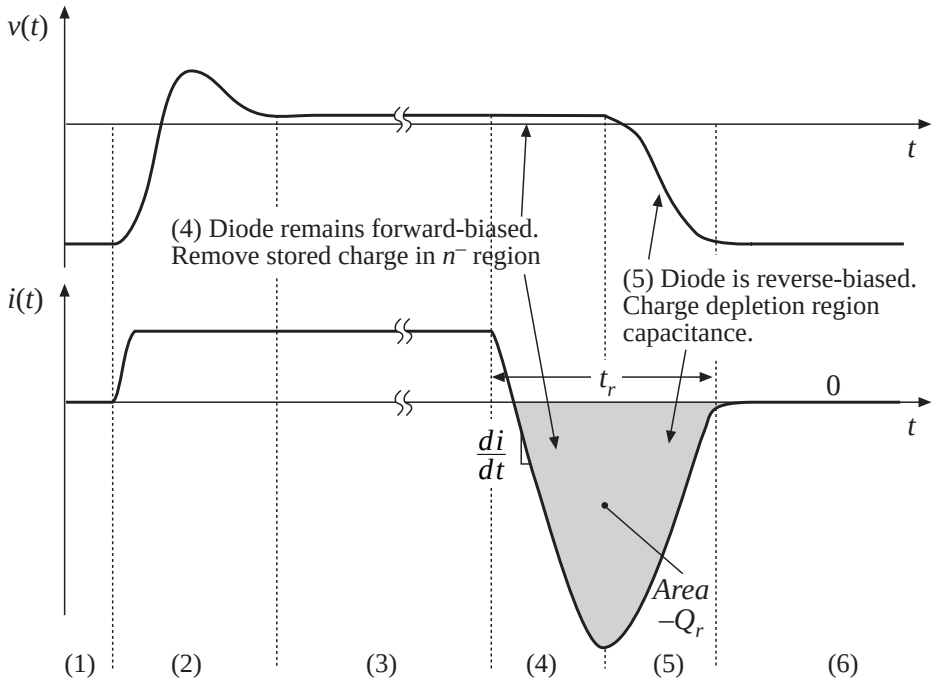
The current $i(t)$ is determined by the converter circuit. This current supplies:

- charge to increase voltage across depletion region
- charge needed to support the on-state current
- charge to reduce on-resistance of n^- region

Turn-off transient

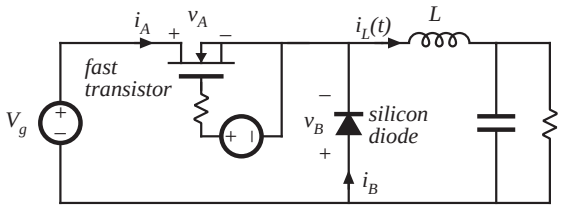


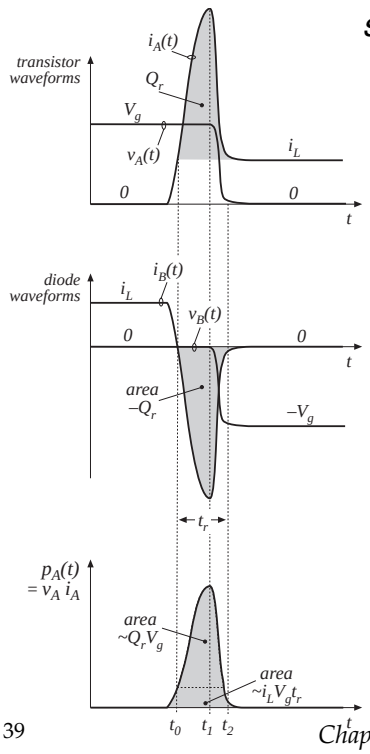
Diode turn-off transient
continued



The diode switching transients induce switching loss in the transistor

see Section 4.3.2





- Diode recovered stored charge Q_r flows through transistor during transistor turn-on transition, inducing switching loss
- Q_r depends on diode on-state forward current, and on the rate-of-change of diode current during diode turn-off transition

Switching loss calculation

Energy lost in transistor:

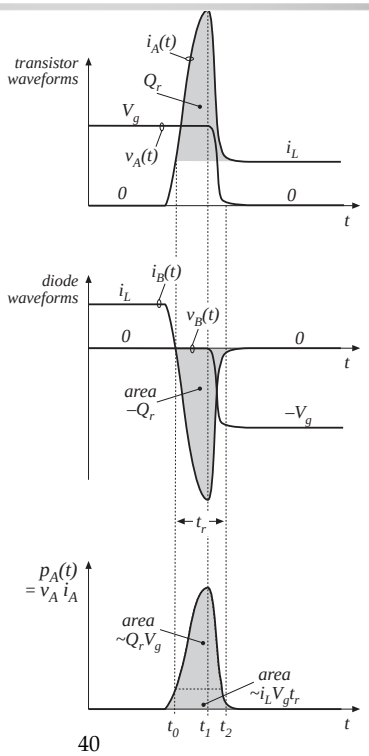
$$W_D = \int_{\substack{\text{switching} \\ \text{transition}}} v_A(t)\, i_A(t)\, dt$$

With abrupt-recovery diode:

$$W_D \approx \int_{\substack{\text{switching} \\ \text{transition}}} V_g\, (i_L - i_B(t))\, dt$$

$$= V_g\, i_L\, t_r + V_g\, Q_r$$

- *Often, this is the largest component of switching loss*



Soft-recovery diode:

$(t_2 - t_1) >> (t_1 - t_0)$

Abrupt-recovery diode:

$(t_2 - t_1) << (t_1 - t_0)$

Types of power diodes

Standard recovery

Reverse recovery time not specified, intended for 50/60Hz

Fast recovery and ultra-fast recovery

Reverse recovery time and recovered charge specified

Intended for converter applications

Schottky diode

A majority carrier device

Essentially no recovered charge

Model with equilibrium *i-v* characteristic, in parallel with depletion region capacitance

Restricted to low voltage (few devices can block 100V or more)

Characteristics of several commercial power rectifier diodes

Part number	*Rated max voltage*	*Rated avg current*	V_F *(typical)*	t_r *(max)*
Fast recovery rectifiers				
1N3913	400V	30A	1.1V	400ns
SD453N25S20PC	2500V	400A	2.2V	2μs
Ultra-fast recovery rectifiers				
MUR815	150V	8A	0.975V	35ns
MUR1560	600V	15A	1.2V	60ns
RHRU100120	1200V	100A	2.6V	60ns
Schottky rectifiers				
MBR6030L	30V	60A	0.48V	
444CNQ045	45V	440A	0.69V	
30CPQ150	150V	30A	1.19V	

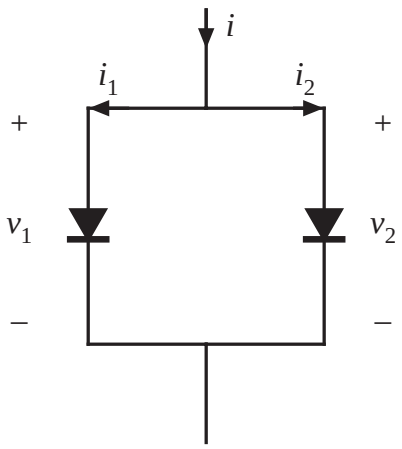
Paralleling diodes

Attempts to parallel diodes, and share the current so that $i_1 = i_2 = i/2$, generally don't work.

Reason: thermal instability caused by temperature dependence of the diode equation.

Increased temperature leads to increased current, or reduced voltage.

One diode will hog the current.

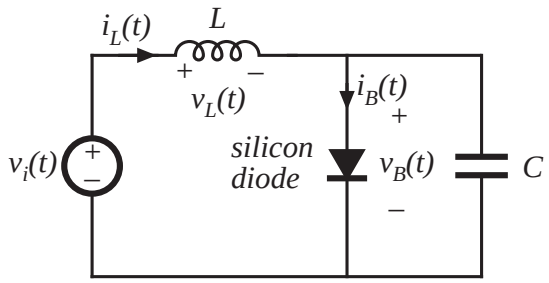


To get the diodes to share the current, heroic measures are required:

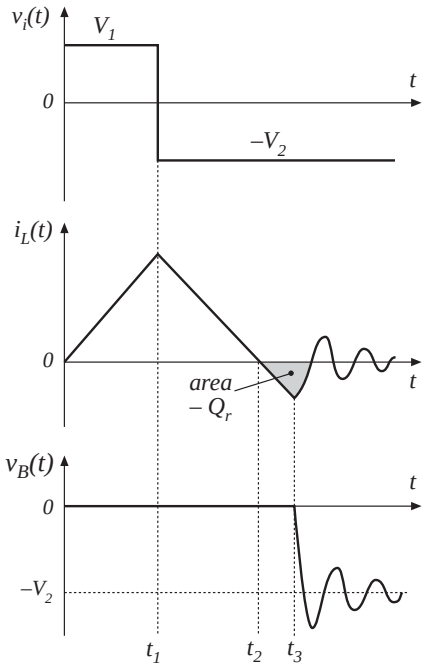
- Select matched devices
- Package on common thermal substrate
- Build external circuitry that forces the currents to balance

Ringing induced by diode stored charge

see Section 4.3.3



- Diode is forward-biased while $i_L(t) > 0$
- Negative inductor current removes diode stored charge Q_r
- When diode becomes reverse-biased, negative inductor current flows through capacitor C.
- Ringing of L-C network is damped by parasitic losses. Ringing energy is lost.



Energy associated with ringing

Recovered charge is $$Q_r = -\int_{t_2}^{t_3} i_L(t)\, dt$$

Energy stored in inductor during interval $t_2 \le t \le t_3$:

$$W_L = \int_{t_2}^{t_3} v_L(t)\, i_L(t)\, dt$$

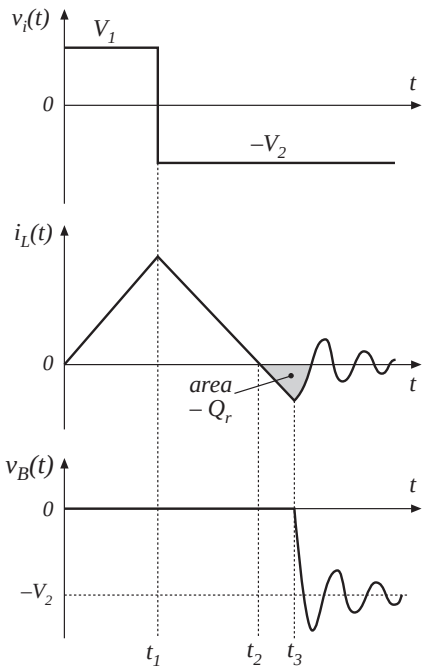
Applied inductor voltage during interval $t_2 \le t \le t_3$:

$$v_L(t) = L\, \frac{di_L(t)}{dt} = -V_2$$

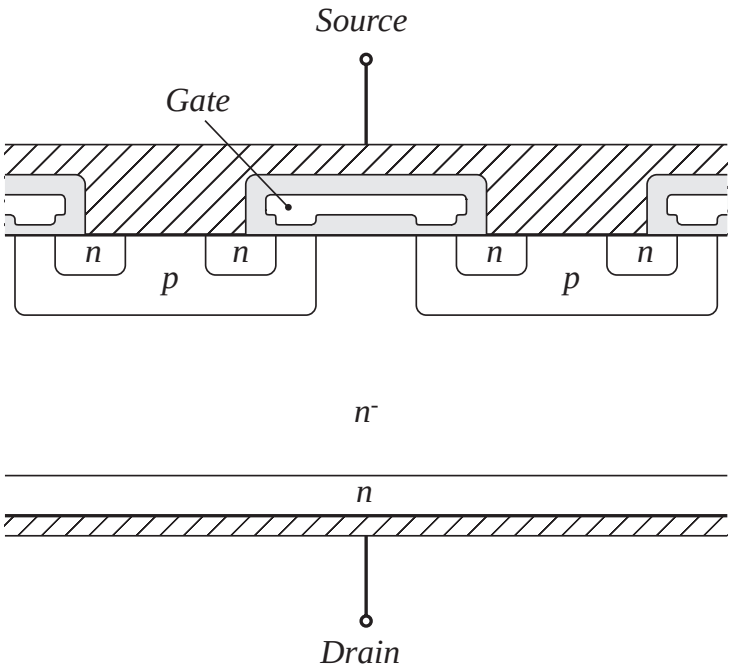
Hence,

$$W_L = \int_{t_2}^{t_3} L\, \frac{di_L(t)}{dt}\, i_L(t)\, dt = \int_{t_2}^{t_3} (-V_2)\, i_L(t)\, dt$$

$$W_L = \tfrac{1}{2} L\, i_L^2(t_3) = V_2\, Q_r$$

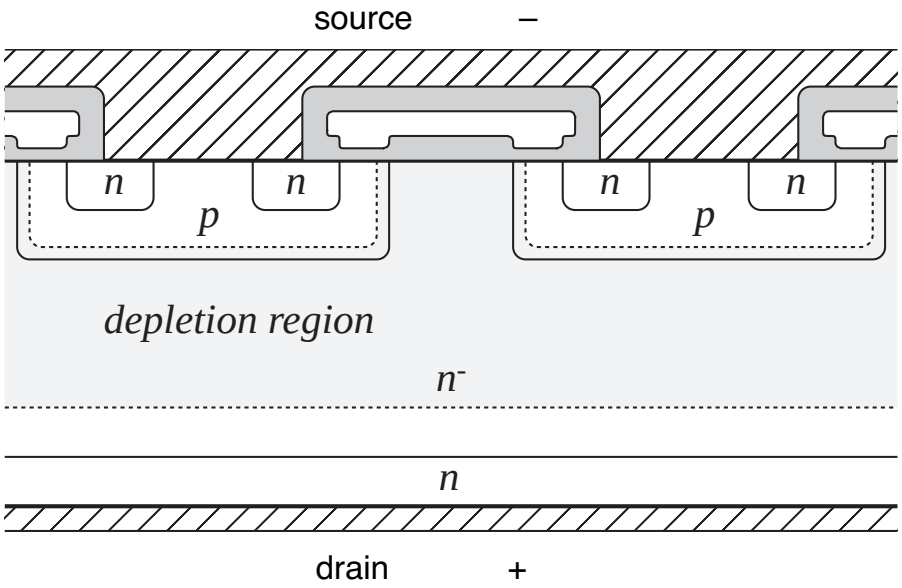


4.2.2. The Power MOSFET



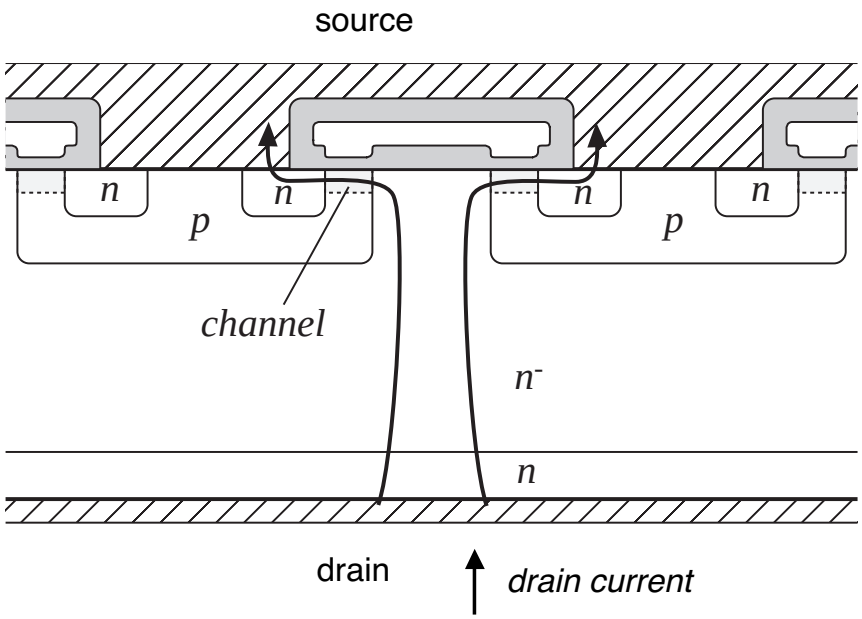
- Gate lengths approaching one micron
- Consists of many small enhancement-mode parallel-connected MOSFET cells, covering the surface of the silicon wafer
- Vertical current flow
- n-channel device is shown

MOSFET: Off state



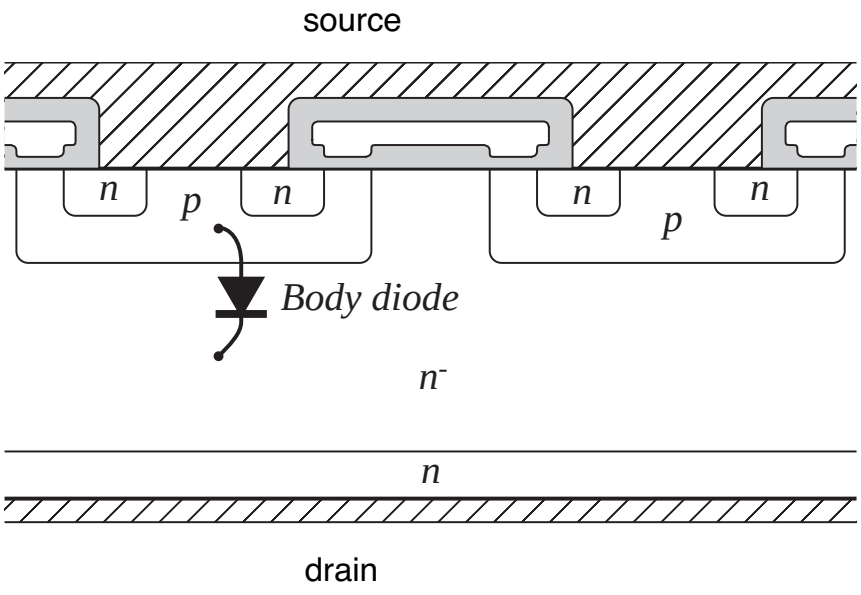
- p-n^- junction is reverse-biased
- off-state voltage appears across n^- region

MOSFET: on state



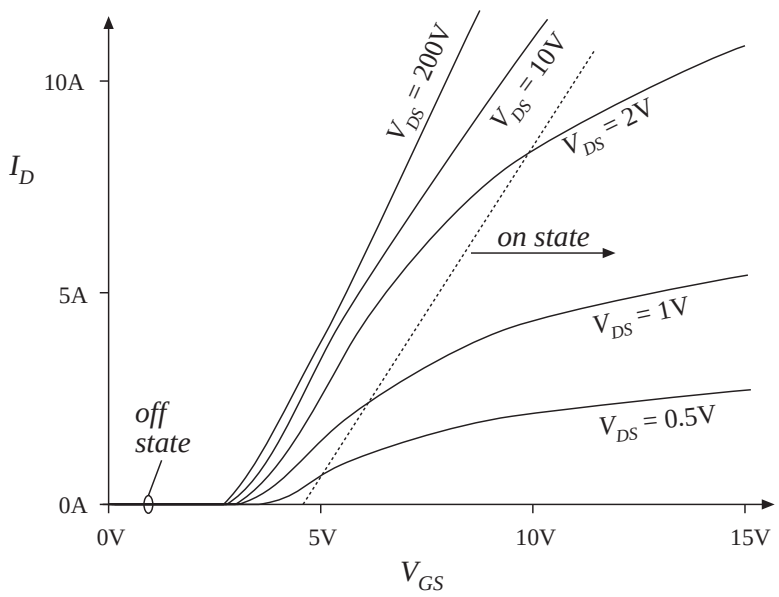
- p-n^- junction is slightly reverse-biased
- positive gate voltage induces conducting channel
- drain current flows through n^- region and conducting channel
- on resistance = total resistances of n^- region, conducting channel, source and drain contacts, etc.

MOSFET body diode



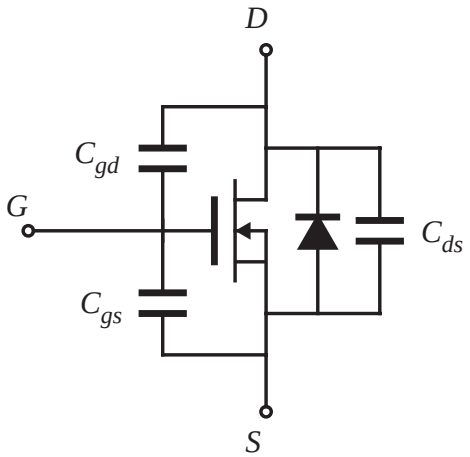
- p-n^- junction forms an effective diode, in parallel with the channel
- negative drain-to-source voltage can forward-bias the body diode
- diode can conduct the full MOSFET rated current
- diode switching speed not optimized —body diode is slow, Q_r is large

Typical MOSFET characteristics



- Off state: $V_{GS} < V_{th}$
- On state: $V_{GS} >> V_{th}$
- MOSFET can conduct peak currents well in excess of average current rating —characteristics are unchanged
- on-resistance has positive temperature coefficient, hence easy to parallel

A simple MOSFET equivalent circuit

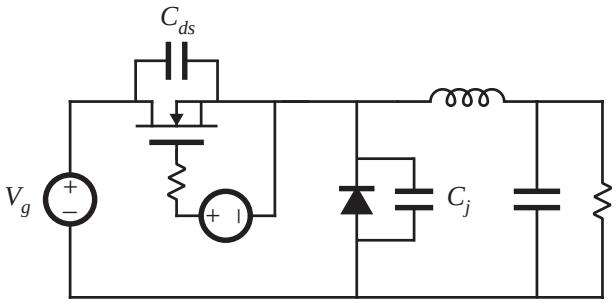


- C_{gs} : large, essentially constant
- C_{gd} : small, highly nonlinear
- C_{ds} : intermediate in value, highly nonlinear
- switching times determined by rate at which gate driver charges/discharges C_{gs} and C_{gd}

$$C_{ds}(v_{ds}) = \frac{C_0}{\sqrt{1 + \frac{v_{ds}}{V_0}}} \qquad C_{ds}(v_{ds}) \approx C_0 \sqrt{\frac{V_0}{v_{ds}}} = \frac{C_0'}{\sqrt{v_{ds}}}$$

Switching loss caused by semiconductor output capacitances

Buck converter example



Energy lost during MOSFET turn-on transition (assuming linear capacitances):

$$W_C = \tfrac{1}{2}\,(C_{ds} + C_j)\,V_g^2$$

MOSFET nonlinear C_{ds}

Approximate dependence of incremental C_{ds} on v_{ds} :

$$C_{ds}(v_{ds}) \approx C_0 \sqrt{\frac{V_0}{v_{ds}}} = \frac{C_0^{'}}{\sqrt{v_{ds}}}$$

Energy stored in C_{ds} at $v_{ds} = V_{DS}$:

$$W_{Cds} = \int v_{ds}\, i_C\, dt = \int_0^{V_{DS}} v_{ds}\, C_{ds}(v_{ds})\, dv_{ds}$$

$$W_{Cds} = \int_0^{V_{DS}} C_0^{'}(v_{ds})\, \sqrt{v_{ds}}\, dv_{ds} = \tfrac{2}{3}\, C_{ds}(V_{DS})\, V_{DS}^2$$

— same energy loss as linear capacitor having value $\tfrac{4}{3}\, C_{ds}(V_{DS})$

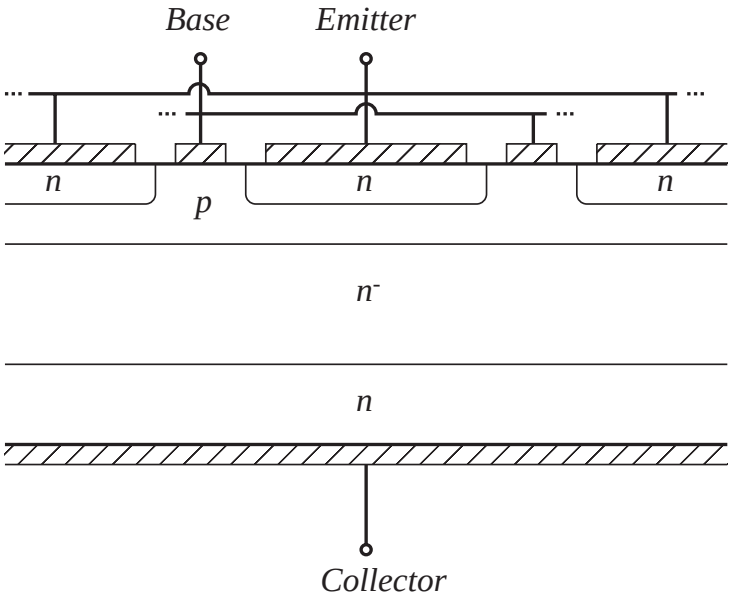
Characteristics of several commercial power MOSFETs

Part number	*Rated max voltage*	*Rated avg current*	R_{on}	Q_g *(typical)*
IRFZ48	60V	50A	0.018Ω	110nC
IRF510	100V	5.6A	0.54Ω	8.3nC
IRF540	100V	28A	0.077Ω	72nC
APT10M25BNR	100V	75A	0.025Ω	171nC
IRF740	400V	10A	0.55Ω	63nC
MTM15N40E	400V	15A	0.3Ω	110nC
APT5025BN	500V	23A	0.25Ω	83nC
APT1001RBNR	1000V	11A	1.0Ω	150nC

MOSFET: conclusions

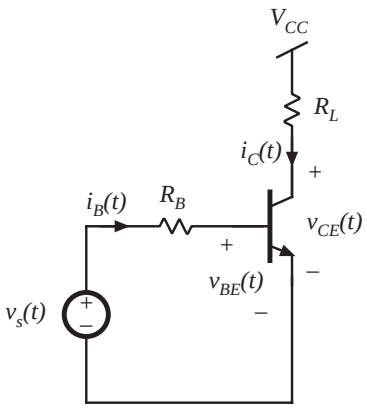
- A majority-carrier device: fast switching speed
- Typical switching frequencies: tens and hundreds of kHz
- On-resistance increases rapidly with rated blocking voltage
- Easy to drive
- The device of choice for blocking voltages less than 500V
- 1000V devices are available, but are useful only at low power levels (100W)
- Part number is selected on the basis of on-resistance rather than current rating

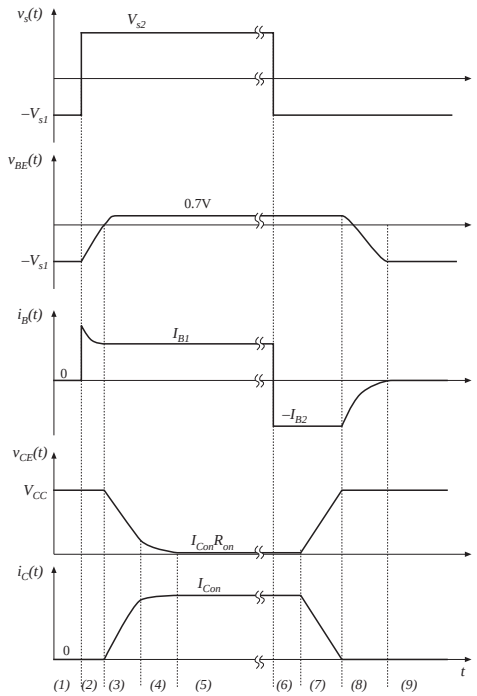
4.2.3. Bipolar Junction Transistor (BJT)



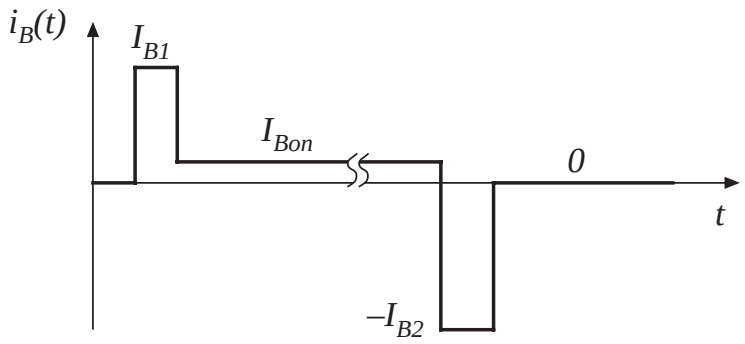
- Interdigitated base and emitter contacts
- Vertical current flow
- npn device is shown
- minority carrier device
- on-state: base-emitter and collector-base junctions are both forward-biased
- on-state: substantial minority charge in p and n^- regions, conductivity modulation

BJT switching times

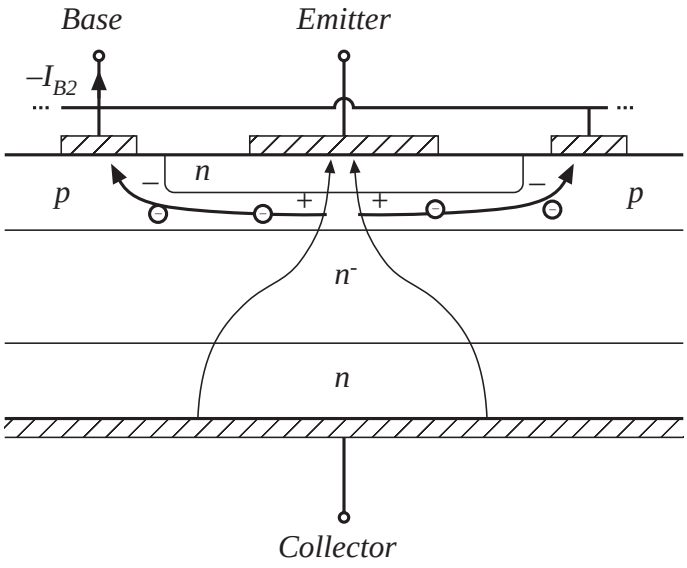




Ideal base current waveform

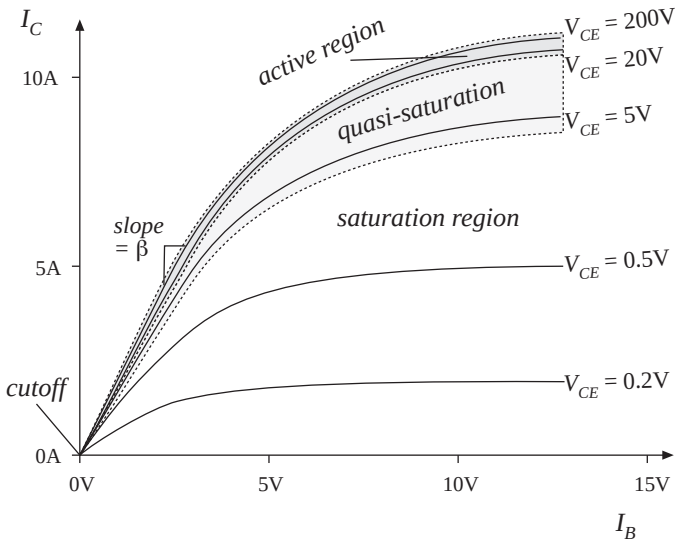


Current crowding due to excessive I_{B2}



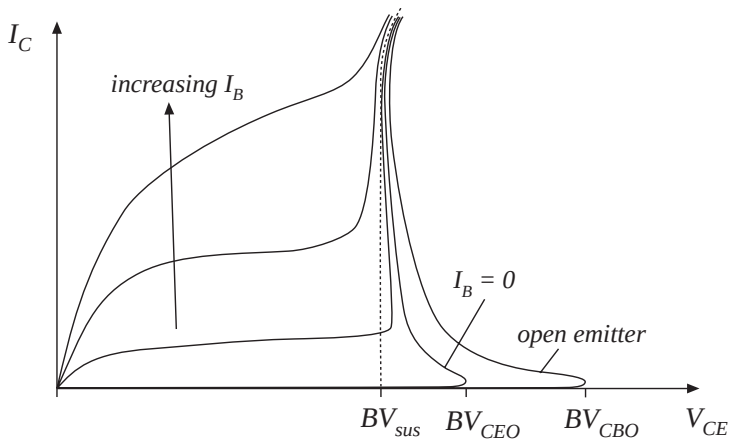
can lead to formation of hot spots and device failure

BJT characteristics



- Off state: $I_B = 0$
- On state: $I_B > I_C / \beta$
- Current gain β decreases rapidly at high current. Device should not be operated at instantaneous currents exceeding the rated value

Breakdown voltages



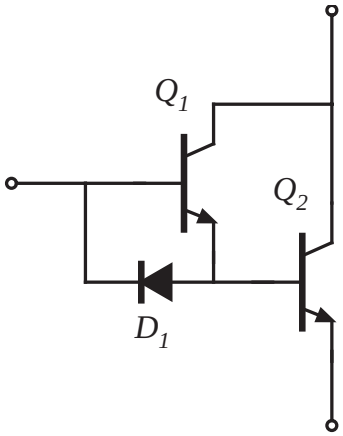
BV_{CBO}: avalanche breakdown voltage of base-collector junction, with the emitter open-circuited

BV_{CEO}: collector-emitter breakdown voltage with zero base current

BV_{sus}: breakdown voltage observed with positive base current

In most applications, the off-state transistor voltage must not exceed BV_{CEO}.

Darlington-connected BJT

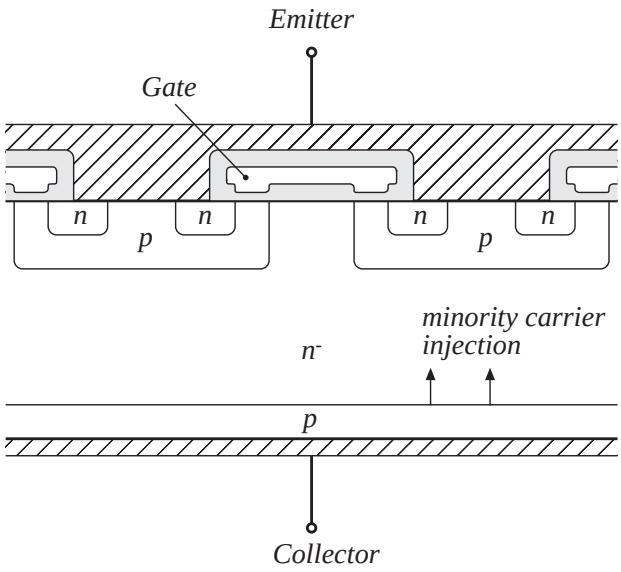


- Increased current gain, for high-voltage applications
- In a monolithic Darlington device, transistors Q_1 and Q_2 are integrated on the same silicon wafer
- Diode D_1 speeds up the turn-off process, by allowing the base driver to actively remove the stored charge of both Q_1 and Q_2 during the turn-off transition

Conclusions: BJT

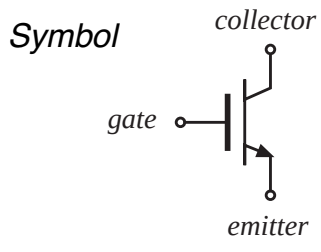
- BJT has been replaced by MOSFET in low-voltage (<500V) applications
- BJT is being replaced by IGBT in applications at voltages above 500V
- A minority-carrier device: compared with MOSFET, the BJT exhibits slower switching, but lower on-resistance at high voltages

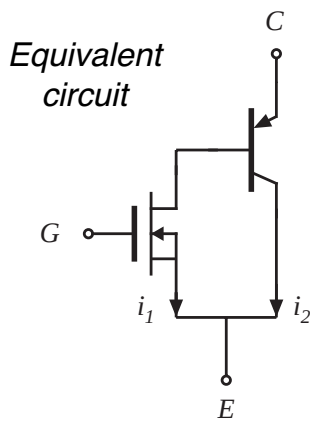
4.2.4. The Insulated Gate Bipolar Transistor (IGBT)



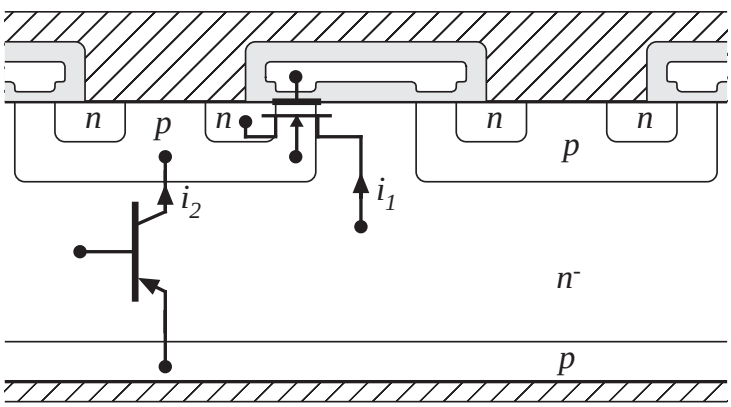
- A four-layer device
- Similar in construction to MOSFET, except extra *p* region
- On-state: minority carriers are injected into n^- region, leading to conductivity modulation
- compared with MOSFET: slower switching times, lower on-resistance, useful at higher voltages (up to 1700V)

The IGBT

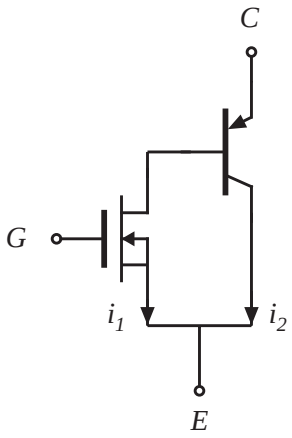


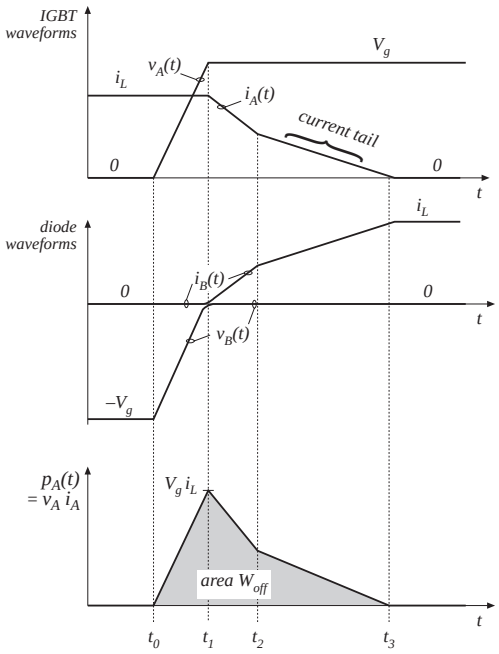


Location of equivalent devices

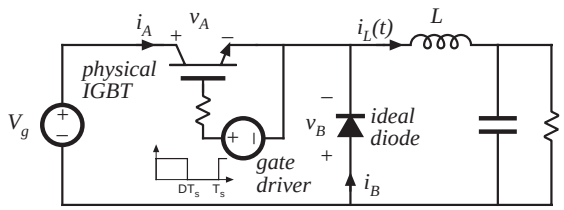


Current tailing in IGBTs

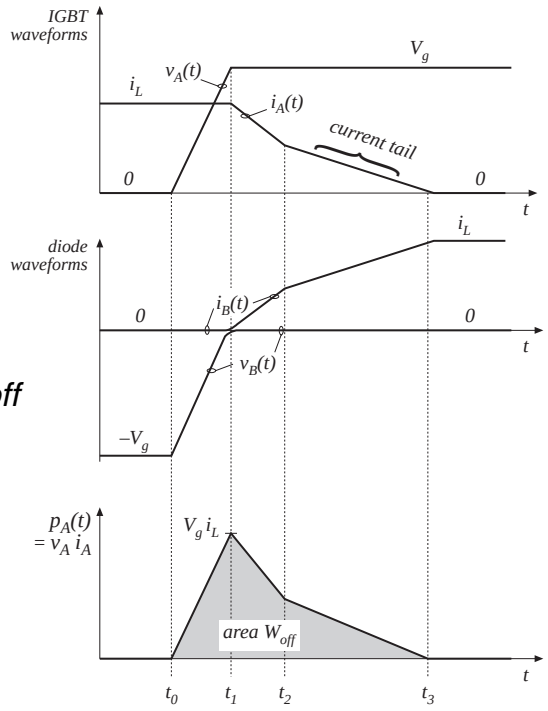




Switching loss due to current-tailing in IGBT



Example: buck converter with IGBT



transistor turn-off transition

$$P_{sw} = \frac{1}{T_s} \int_{\substack{\text{switching} \\ \text{transitions}}} p_A(t)\, dt = (W_{on} + W_{off})\, f_s$$

Characteristics of several commercial devices

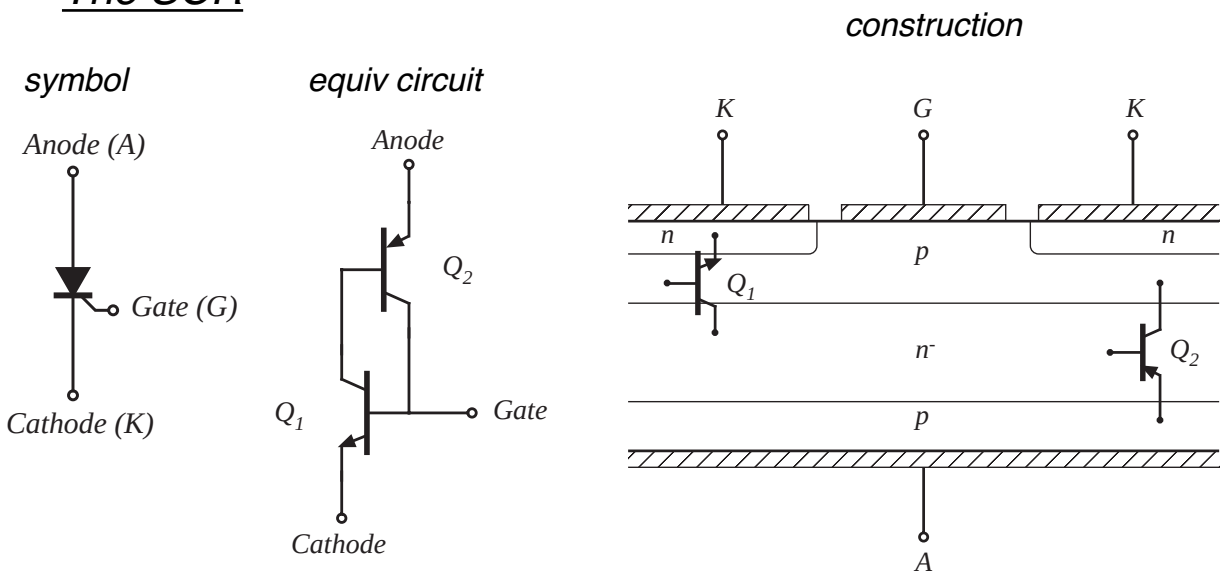
Part number	*Rated max voltage*	*Rated avg current*	V_F *(typical)*	t_f *(typical)*
Single-chip devices				
HGTG32N60E2	600V	32A	2.4V	0.62μs
HGTG30N120D2	1200V	30A	3.2A	0.58μs
Multiple-chip power modules				
CM400HA-12E	600V	400A	2.7V	0.3μs
CM300HA-24E	1200V	300A	2.7V	0.3μs

Conclusions: IGBT

- Becoming the device of choice in 500 to 1700V+ applications, at power levels of 1-1000kW
- Positive temperature coefficient at high current —easy to parallel and construct modules
- Forward voltage drop: diode in series with on-resistance. 2-4V typical
- Easy to drive —similar to MOSFET
- Slower than MOSFET, but faster than Darlington, GTO, SCR
- Typical switching frequencies: 3-30kHz
- IGBT technology is rapidly advancing:
  - 3300 V devices: HVIGBTs
  - 150 kHz switching frequencies in 600 V devices

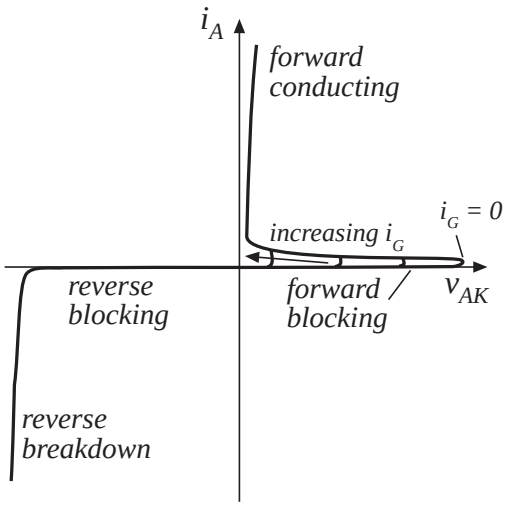
4.2.5. Thyristors (SCR, GTO, MCT)

The SCR



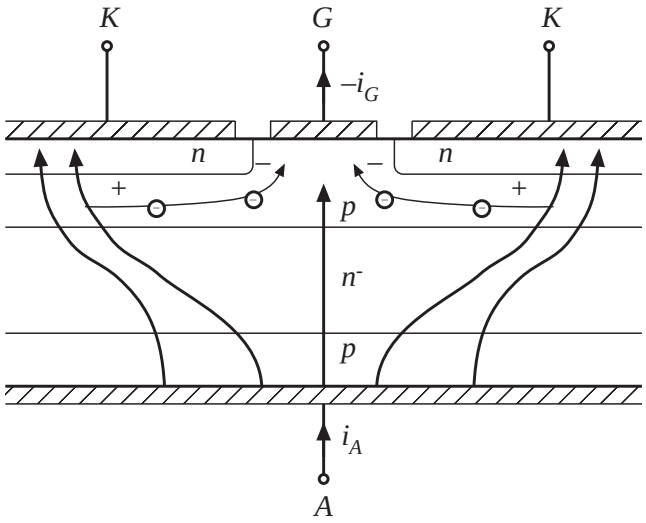
The Silicon Controlled Rectifier (SCR)

- Positive feedback —a latching device
- A minority carrier device
- Double injection leads to very low on-resistance, hence low forward voltage drops attainable in very high voltage devices
- Simple construction, with large feature size
- Cannot be actively turned off
- A voltage-bidirectional two-quadrant switch
- 5000-6000V, 1000-2000A devices



Why the conventional SCR cannot be turned off via gate control

- Large feature size
- Negative gate current induces lateral voltage drop along gate-cathode junction
- Gate-cathode junction becomes reverse-biased only in vicinity of gate contact



The Gate Turn-Off Thyristor (GTO)

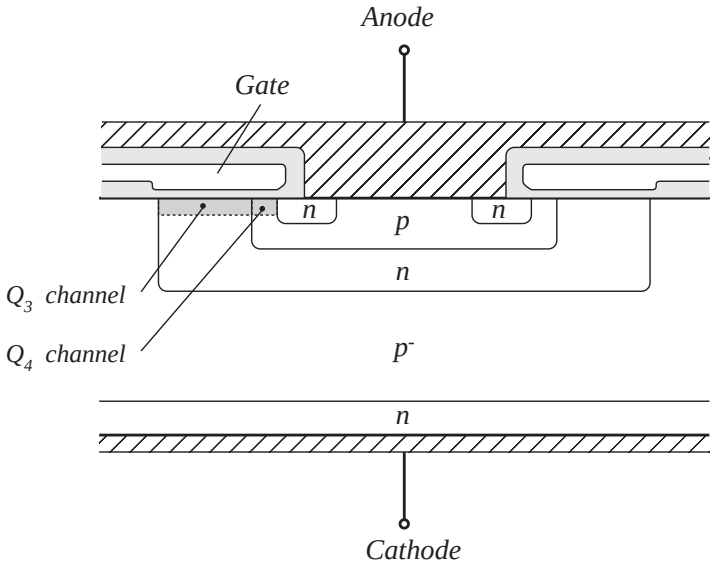
- An SCR fabricated using modern techniques —small feature size
- Gate and cathode contacts are highly interdigitated
- Negative gate current is able to completely reverse-bias the gate-cathode junction

Turn-off transition:

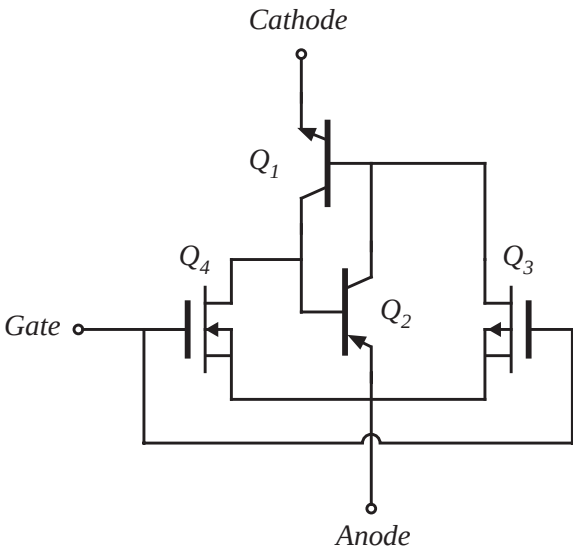
- Turn-off current gain: typically 2-5
- Maximum controllable on-state current: maximum anode current that can be turned off via gate control. GTO can conduct peak currents well in excess of average current rating, but cannot switch off

The MOS-Controlled Thyristor (MCT)

- Still an emerging device, but some devices are commercially available
- p-type device
- A latching SCR, with added built-in MOSFETs to assist the turn-on and turn-off processes
- Small feature size, highly interdigitated, modern fabrication



The MCT: equivalent circuit



- Negative gate-anode voltage turns p-channel MOSFET Q_3 on, causing Q_1 and Q_2 to latch ON
- Positive gate-anode voltage turns n-channel MOSFET Q_4 on, reverse-biasing the base-emitter junction of Q_2 and turning off the device
- Maximum current that can be interrupted is limited by the on-resistance of Q_4

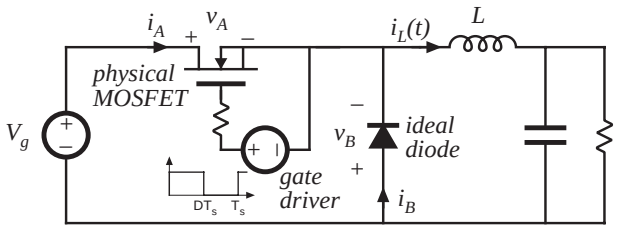
Summary: Thyristors

- The thyristor family: double injection yields lowest forward voltage drop in high voltage devices. More difficult to parallel than MOSFETs and IGBTs
- The SCR: highest voltage and current ratings, low cost, passive turn-off transition
- The GTO: intermediate ratings (less than SCR, somewhat more than IGBT). Slower than IGBT. Slower than MCT. Difficult to drive.
- The MCT: So far, ratings lower than IGBT. Slower than IGBT. Easy to drive. Second breakdown problems? Still an emerging device.

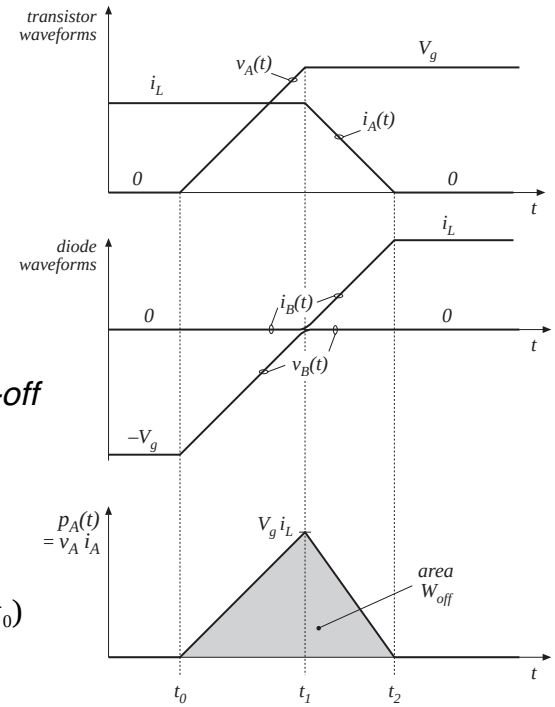
4.3. Switching loss

- Energy is lost during the semiconductor switching transitions, via several mechanisms:
  - Transistor switching times
  - Diode stored charge
  - Energy stored in device capacitances and parasitic inductances
- Semiconductor devices are *charge controlled*
- Time required to insert or remove the controlling charge determines switching times

4.3.1. Transistor switching with clamped inductive load



Buck converter example



$v_B(t) = v_A(t) - V_g$

$i_A(t) + i_B(t) = i_L$

transistor turn-off transition

$$W_{off} = \tfrac{1}{2}\, V_g i_L\, (t_2 - t_0)$$

Switching loss induced by transistor turn-off transition

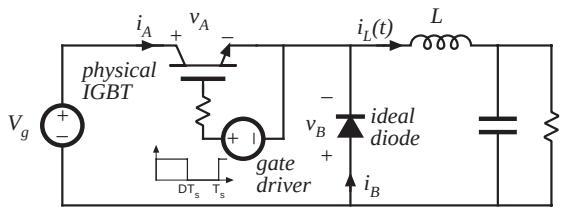
Energy lost during transistor turn-off transition:

$$W_{off} = \tfrac{1}{2}\, V_g i_L\, (t_2 - t_0)$$

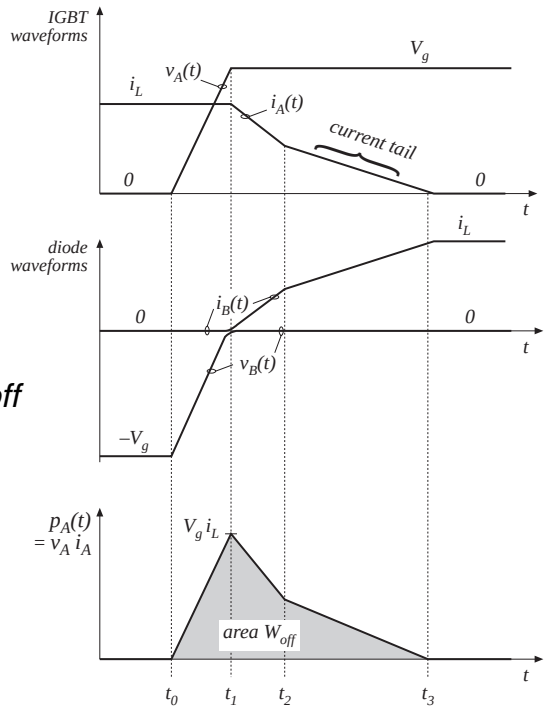
Similar result during transistor turn-on transition.
Average power loss:

$$P_{sw} = \frac{1}{T_s} \int_{\substack{\text{switching} \\ \text{transitions}}} p_A(t)\, dt = (W_{on} + W_{off})\, f_s$$

Switching loss due to current-tailing in IGBT



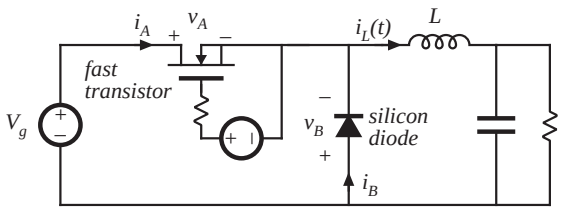
Example: buck converter with IGBT



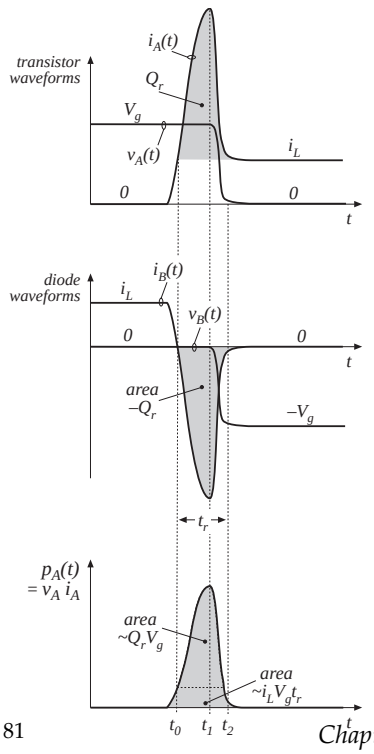
transistor turn-off transition

$$P_{sw} = \frac{1}{T_s} \int_{\substack{\text{switching} \\ \text{transitions}}} p_A(t)\, dt = (W_{on} + W_{off})\, f_s$$

4.3.2. Diode recovered charge



- Diode recovered stored charge Q_r flows through transistor during transistor turn-on transition, inducing switching loss
- Q_r depends on diode on-state forward current, and on the rate-of-change of diode current during diode turn-off transition



Switching loss calculation

Energy lost in transistor:

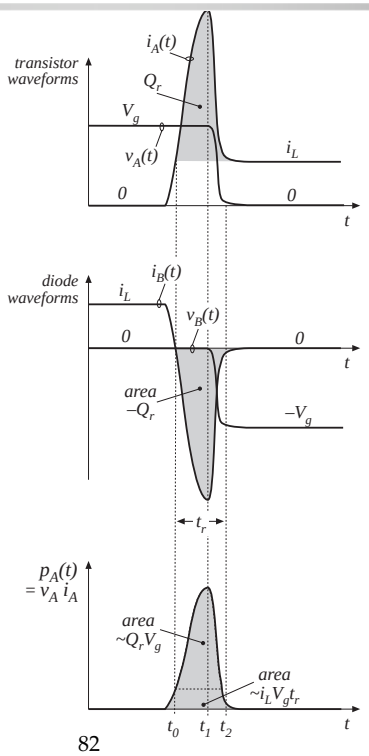
$$W_D = \int_{\substack{\text{switching}\\ \text{transition}}} v_A(t)\, i_A(t)\, dt$$

With abrupt-recovery diode:

$$W_D \approx \int_{\substack{\text{switching}\\ \text{transition}}} V_g\, (i_L - i_B(t))\, dt$$

$$= V_g\, i_L\, t_r + V_g\, Q_r$$

- *Often, this is the largest component of switching loss*



Soft-recovery diode:

$(t_2 - t_1) >> (t_1 - t_0)$

Abrupt-recovery diode:

$(t_2 - t_1) << (t_1 - t_0)$

4.3.3. Device capacitances, and leakage, package, and stray inductances

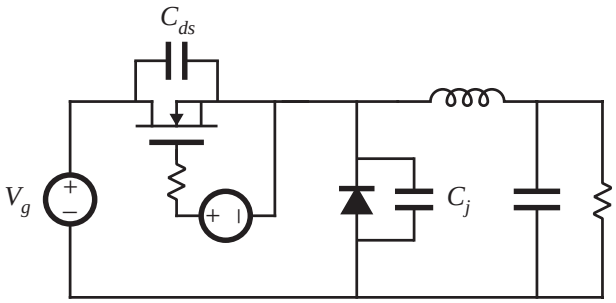
- Capacitances that appear effectively in parallel with switch elements are shorted when the switch turns on. Their stored energy is lost during the switch turn-on transition.
- Inductances that appear effectively in series with switch elements are open-circuited when the switch turns off. Their stored energy is lost during the switch turn-off transition.

Total energy stored in linear capacitive and inductive elements:

$$W_C = \sum_{\substack{\text{capacitive}\\ \text{elements}}} \tfrac{1}{2} C_i V_i^2 \qquad W_L = \sum_{\substack{\text{inductive}\\ \text{elements}}} \tfrac{1}{2} L_j I_j^2$$

Example: semiconductor output capacitances

Buck converter example



Energy lost during MOSFET turn-on transition (assuming linear capacitances):

$$W_C = \tfrac{1}{2}\,(C_{ds} + C_j)\,V_g^2$$

MOSFET nonlinear C_{ds}

Approximate dependence of incremental C_{ds} on v_{ds} :

$$C_{ds}(v_{ds}) \approx C_0 \sqrt{\frac{V_0}{v_{ds}}} = \frac{C_0^{'}}{\sqrt{v_{ds}}}$$

Energy stored in C_{ds} at $v_{ds} = V_{DS}$:

$$W_{Cds} = \int v_{ds}\, i_C\, dt = \int_0^{V_{DS}} v_{ds}\, C_{ds}(v_{ds})\, dv_{ds}$$

$$W_{Cds} = \int_0^{V_{DS}} C_0^{'}(v_{ds})\, \sqrt{v_{ds}}\, dv_{ds} = \tfrac{2}{3}\, C_{ds}(V_{DS})\, V_{DS}^2$$

— same energy loss as linear capacitor having value $\tfrac{4}{3}\, C_{ds}(V_{DS})$

Some other sources of this type of switching loss

Schottky diode

- Essentially no stored charge
- Significant reverse-biased junction capacitance

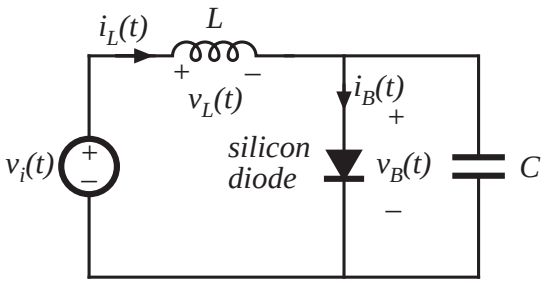
Transformer leakage inductance

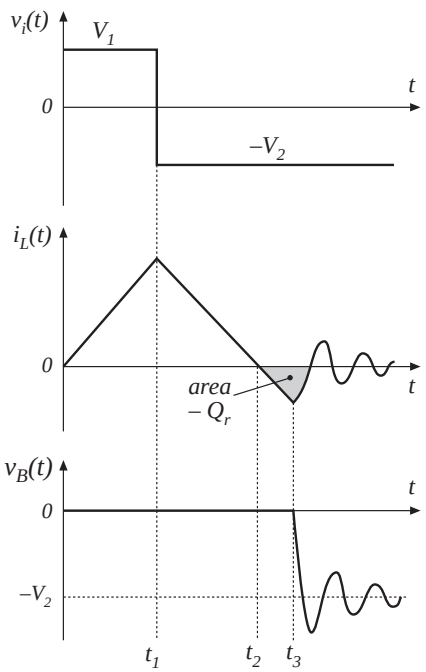
- Effective inductances in series with windings
- A significant loss when windings are not tightly coupled

Interconnection and package inductances

- Diodes
- Transistors
- A significant loss in high current applications

Ringing induced by diode stored charge





- Diode is forward-biased while $i_L(t) > 0$
- Negative inductor current removes diode stored charge Q_r
- When diode becomes reverse-biased, negative inductor current flows through capacitor C.
- Ringing of L-C network is damped by parasitic losses. Ringing energy is lost.

Energy associated with ringing

Recovered charge is $Q_r = -\int_{t_2}^{t_3} i_L(t)\,dt$

Energy stored in inductor during interval $t_2 \le t \le t_3$:

$$W_L = \int_{t_2}^{t_3} v_L(t)\, i_L(t)\,dt$$

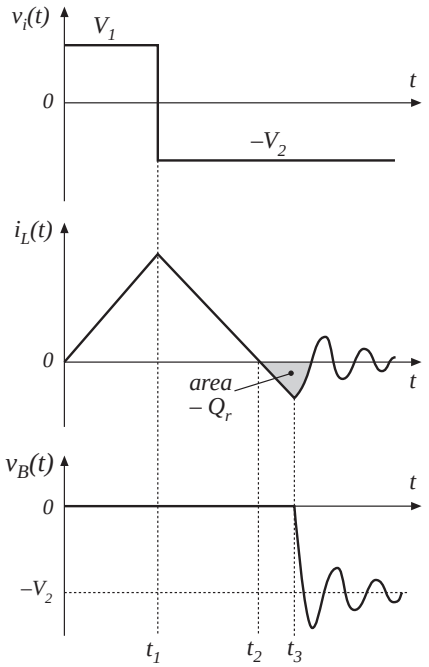
Applied inductor voltage during interval $t_2 \le t \le t_3$:

$$v_L(t) = L\,\frac{di_L(t)}{dt} = -V_2$$

Hence,

$$W_L = \int_{t_2}^{t_3} L\,\frac{di_L(t)}{dt}\, i_L(t)\,dt = \int_{t_2}^{t_3} (-V_2)\, i_L(t)\,dt$$

$$W_L = \tfrac{1}{2} L\, i_L^2(t_3) = V_2\, Q_r$$



4.3.4. Efficiency vs. switching frequency

Add up all of the energies lost during the switching transitions of one switching period:

$$W_{tot} = W_{on} + W_{off} + W_D + W_C + W_L + \ldots$$

Average switching power loss is

$$P_{sw} = W_{tot}\, f_{sw}$$

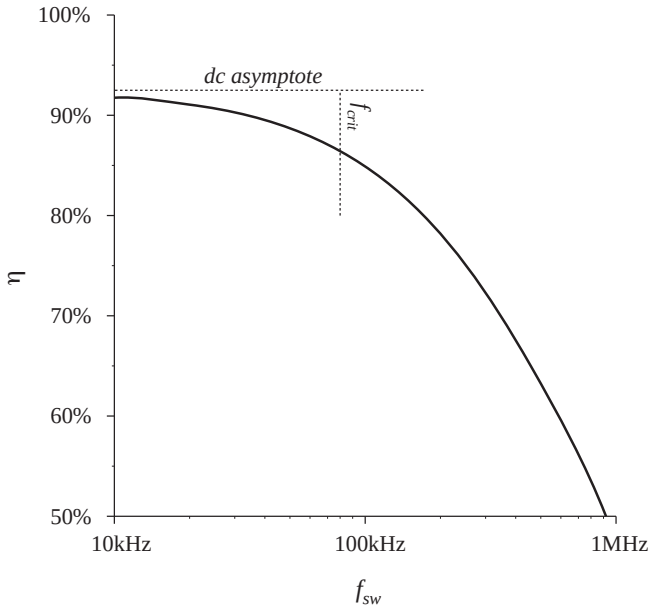
Total converter loss can be expressed as

$$P_{loss} = P_{cond} + P_{fixed} + W_{tot}\, f_{sw}$$

where P_{fixed} = fixed losses (independent of load and f_{sw})
P_{cond} = conduction losses

Efficiency vs. switching frequency

$$P_{loss} = P_{cond} + P_{fixed} + W_{tot}\, f_{sw}$$



Switching losses are equal to the other converter losses at the critical frequency

$$f_{crit} = \frac{P_{cond} + P_{fixed}}{W_{tot}}$$

This can be taken as a rough upper limit on the switching frequency of a practical converter. For $f_{sw} > f_{crit}$, the efficiency decreases rapidly with frequency.

Summary of chapter 4

1. How an SPST ideal switch can be realized using semiconductor devices depends on the polarity of the voltage which the devices must block in the off-state, and on the polarity of the current which the devices must conduct in the on-state.
2. Single-quadrant SPST switches can be realized using a single transistor or a single diode, depending on the relative polarities of the off-state voltage and on-state current.
3. Two-quadrant SPST switches can be realized using a transistor and diode, connected in series (bidirectional-voltage) or in anti-parallel (bidirectional-current). Several four-quadrant schemes are also listed here.
4. A “synchronous rectifier” is a MOSFET connected to conduct reverse current, with gate drive control as necessary. This device can be used where a diode would otherwise be required. If a MOSFET with sufficiently low R_{on} is used, reduced conduction loss is obtained.

Summary of chapter 4

5. Majority carrier devices, including the MOSFET and Schottky diode, exhibit very fast switching times, controlled essentially by the charging of the device capacitances. However, the forward voltage drops of these devices increases quickly with increasing breakdown voltage.
6. Minority carrier devices, including the BJT, IGBT, and thyristor family, can exhibit high breakdown voltages with relatively low forward voltage drop. However, the switching times of these devices are longer, and are controlled by the times needed to insert or remove stored minority charge.
7. Energy is lost during switching transitions, due to a variety of mechanisms. The resulting average power loss, or switching loss, is equal to this energy loss multiplied by the switching frequency. Switching loss imposes an upper limit on the switching frequencies of practical converters.

Summary of chapter 4

8. The diode and inductor present a “clamped inductive load” to the transistor. When a transistor drives such a load, it experiences high instantaneous power loss during the switching transitions. An example where this leads to significant switching loss is the IGBT and the “current tail” observed during its turn-off transition.
9. Other significant sources of switching loss include diode stored charge and energy stored in certain parasitic capacitances and inductances. Parasitic ringing also indicates the presence of switching loss.

Chapter 5. The Discontinuous Conduction Mode

5.1. Origin of the discontinuous conduction mode, and mode boundary

5.2. Analysis of the conversion ratio $M(D,K)$

5.3. Boost converter example

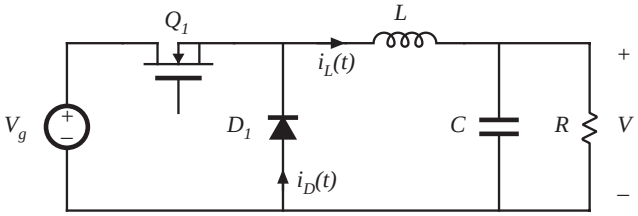
5.4. Summary of results and key points

Introduction to Discontinuous Conduction Mode (DCM)

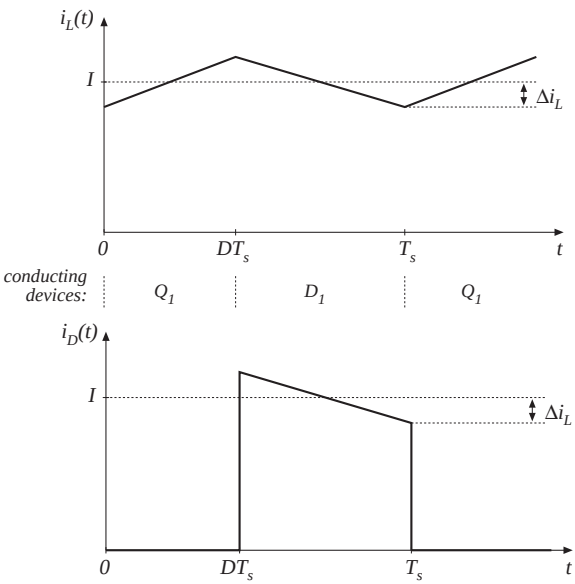
- Occurs because switching ripple in inductor current or capacitor voltage causes polarity of applied switch current or voltage to reverse, such that the current- or voltage-unidirectional assumptions made in realizing the switch are violated.
- Commonly occurs in dc-dc converters and rectifiers, having single-quadrant switches. May also occur in converters having two-quadrant switches.
- Typical example: dc-dc converter operating at light load (small load current). Sometimes, dc-dc converters and rectifiers are purposely designed to operate in DCM at all loads.
- Properties of converters change radically when DCM is entered:
  - M becomes load-dependent
  - Output impedance is increased
  - Dynamics are altered
  - Control of output voltage may be lost when load is removed

5.1. Origin of the discontinuous conduction mode, and mode boundary

Buck converter example, with single-quadrant switches



continuous conduction mode (CCM)



Minimum diode current is $(I - \Delta i_L)$

Dc component $I = V/R$

Current ripple is

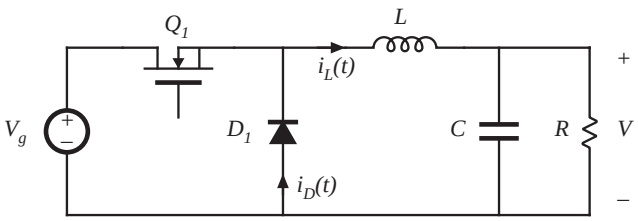
$$\Delta i_L = \frac{(V_g - V)}{2L} DT_s = \frac{V_g DD'T_s}{2L}$$

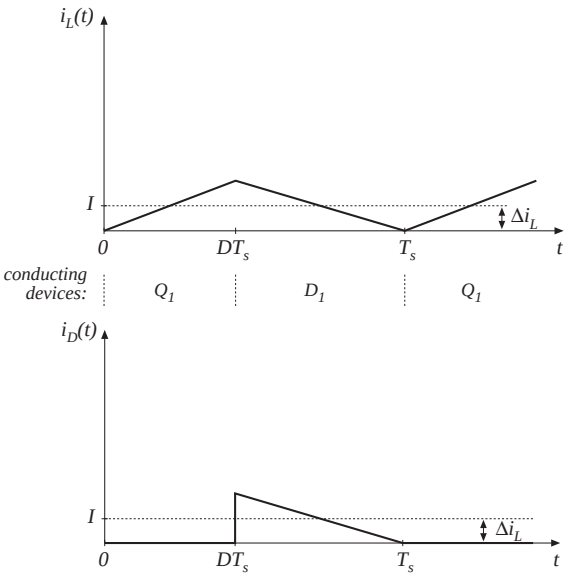
Note that I depends on load, but Δi_L does not.

Reduction of load current

Increase R, until $I = \Delta i_L$

CCM-DCM boundary





Minimum diode current is $(I - \Delta i_L)$

Dc component $I = V/R$

Current ripple is

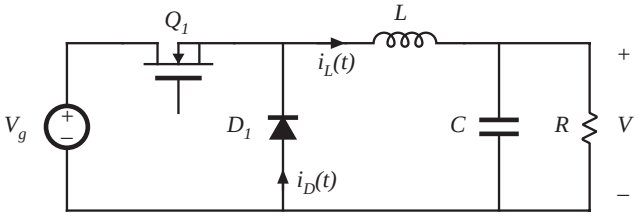
$$\Delta i_L = \frac{(V_g - V)}{2L} DT_s = \frac{V_g DD'T_s}{2L}$$

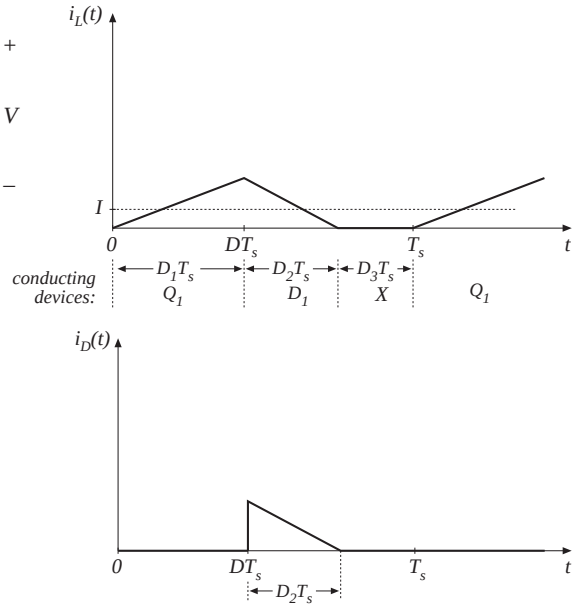
Note that I depends on load, but Δi_L does not.

Further reduce load current

Increase R some more, such that $I < \Delta i_L$

Discontinuous conduction mode





Minimum diode current is $(I - \Delta i_L)$

Dc component $I = V/R$

Current ripple is

$$\Delta i_L = \frac{(V_g - V)}{2L} DT_s = \frac{V_g DD'T_s}{2L}$$

Note that I depends on load, but Δi_L does not.

The load current continues to be positive and non-zero.

Mode boundary

$$I > \Delta i_L \quad \textit{for CCM}$$
$$I < \Delta i_L \quad \textit{for DCM}$$

Insert buck converter expressions for I and Δi_L :

$$\frac{DV_g}{R} < \frac{DD'T_sV_g}{2L}$$

Simplify:

$$\frac{2L}{RT_s} < D'$$

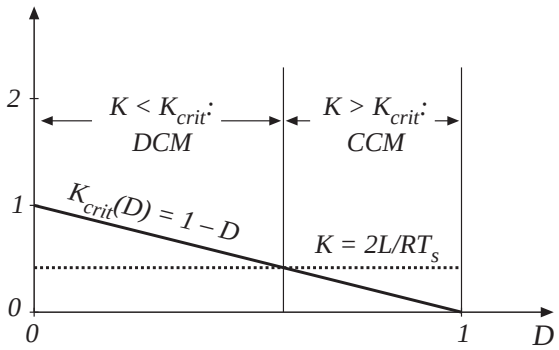
This expression is of the form

$$K < K_{crit}(D) \qquad \textit{for DCM}$$

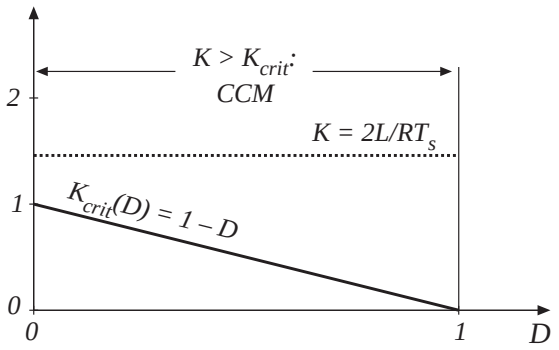
where $K = \frac{2L}{RT_s}$ *and* $K_{crit}(D) = D'$

K and K_{crit} vs. D

for $K < 1$:



for $K > 1$:



Critical load resistance R_{crit}

Solve K_{crit} equation for load resistance R:

$$R < R_{crit}(D) \quad \textit{for CCM}$$
$$R > R_{crit}(D) \quad \textit{for DCM}$$

where $$R_{crit}(D) = \frac{2L}{D'T_s}$$

Summary: mode boundary

$K > K_{crit}(D)$ *or* $R < R_{crit}(D)$ *for CCM*

$K < K_{crit}(D)$ *or* $R > R_{crit}(D)$ *for DCM*

Table 5.1. CCM-DCM mode boundaries for the buck, boost, and buck-boost converters

Converter	$K_{crit}(D)$	$\max_{0 \le D \le 1}(K_{crit})$	$R_{crit}(D)$	$\min_{0 \le D \le 1}(R_{crit})$
Buck	$(1 - D)$	1	$\frac{2L}{(1-D)T_s}$	$2\frac{L}{T_s}$
Boost	$D(1 - D)^2$	$\frac{4}{27}$	$\frac{2L}{D(1-D)^2 T_s}$	$\frac{27}{2}\frac{L}{T_s}$
Buck-boost	$(1 - D)^2$	1	$\frac{2L}{(1-D)^2 T_s}$	$2\frac{L}{T_s}$

5.2. Analysis of the conversion ratio *M(D,K)*

Analysis techniques for the discontinuous conduction mode:

Inductor volt-second balance

$$\langle v_L \rangle = \frac{1}{T_s}\int_0^{T_s} v_L(t)\,dt = 0$$

Capacitor charge balance

$$\langle i_C \rangle = \frac{1}{T_s}\int_0^{T_s} i_C(t)\,dt = 0$$

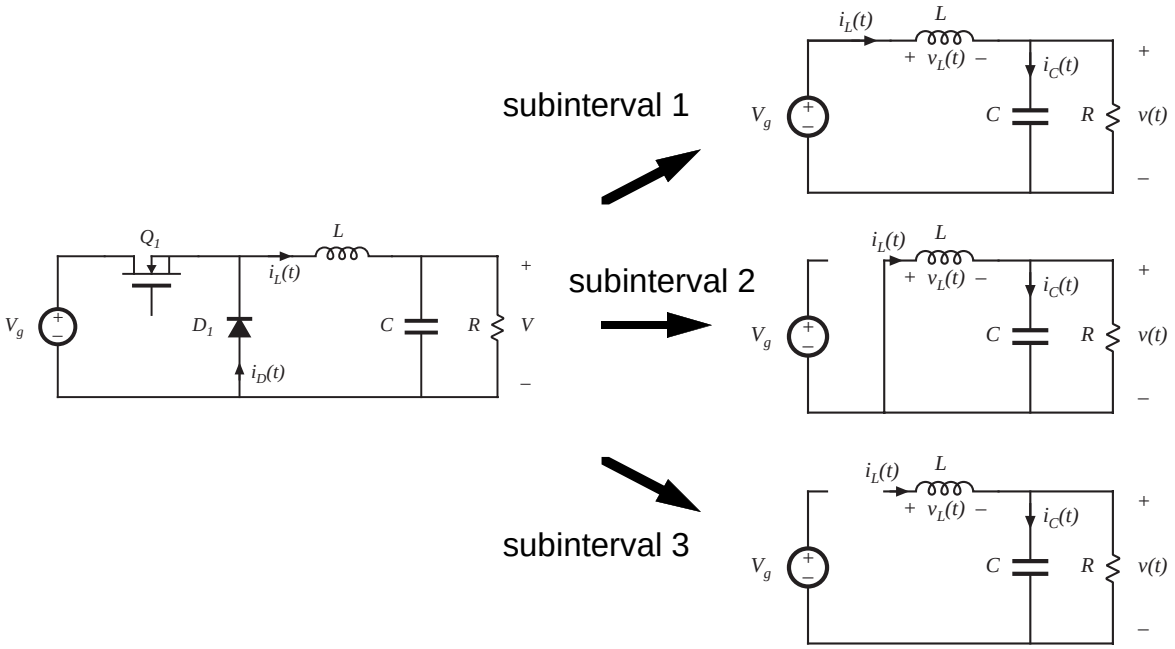
Small ripple approximation sometimes applies:

$v(t) \approx V$ because $\Delta v << V$

$i(t) \approx I$ is a poor approximation when $\Delta i > I$

Converter steady-state equations obtained via charge balance on each capacitor and volt-second balance on each inductor. Use care in applying small ripple approximation.

Example: Analysis of DCM buck converter *M(D,K)*

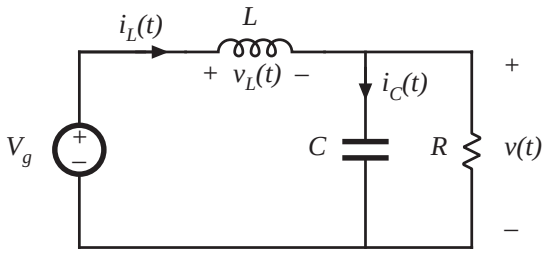


Subinterval 1

$$v_L(t) = V_g - v(t)$$
$$i_C(t) = i_L(t) - v(t) / R$$

Small ripple approximation for *v(t)* (but not for *i(t)*!):

$$v_L(t) \approx V_g - V$$
$$i_C(t) \approx i_L(t) - V / R$$

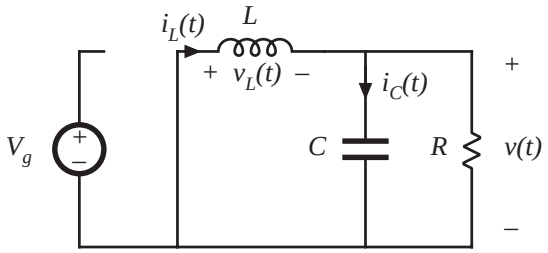


Subinterval 2

$$v_L(t) = -v(t)$$
$$i_C(t) = i_L(t) - v(t) / R$$

Small ripple approximation for *v(t)* but not for *i(t)*:

$$v_L(t) \approx -V$$
$$i_C(t) \approx i_L(t) - V / R$$

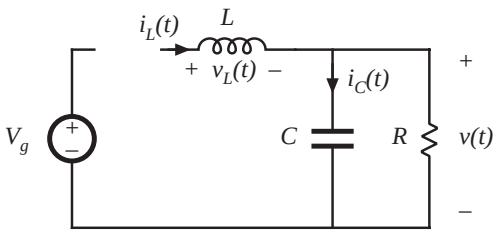


Subinterval 3

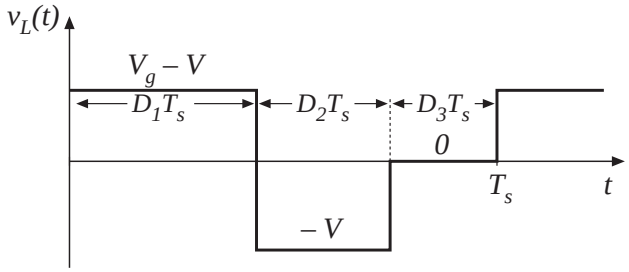
$$v_L = 0, \quad i_L = 0$$
$$i_C(t) = i_L(t) - v(t) / R$$

Small ripple approximation:

$$v_L(t) = 0$$
$$i_C(t) = -V / R$$



Inductor volt-second balance



Volt-second balance:

$$\left\langle v_L(t) \right\rangle = D_1(V_g - V) + D_2(-V) + D_3(0) = 0$$

Solve for V:

$$V = V_g \frac{D_1}{D_1 + D_2}$$

note that D_2 is unknown

Capacitor charge balance

node equation:

$$i_L(t) = i_C(t) + V / R$$

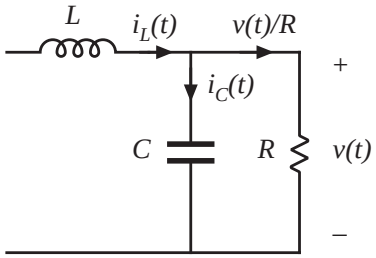
capacitor charge balance:

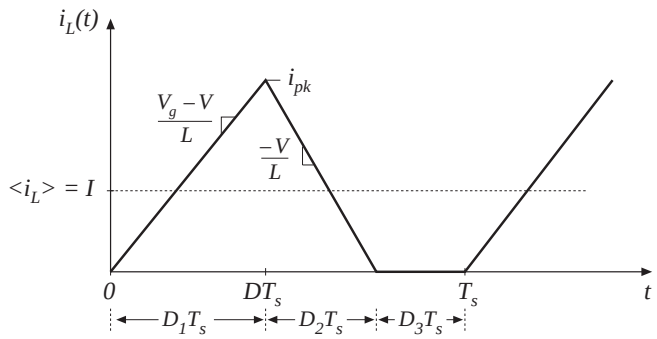
$$\left\langle i_C \right\rangle = 0$$

hence

$$\left\langle i_L \right\rangle = V / R$$

must compute dc component of inductor current and equate to load current (for this buck converter example)





Inductor current waveform

peak current:

$$i_L(D_1T_s) = i_{pk} = \frac{V_g - V}{L} D_1T_s$$

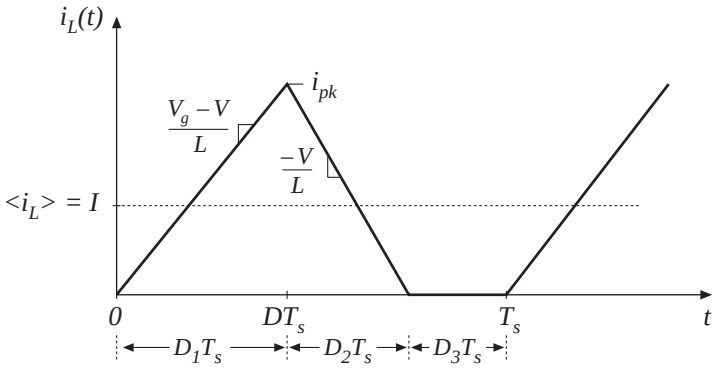
average current:

$$\left\langle i_L \right\rangle = \frac{1}{T_s} \int_0^{T_s} i_L(t)\, dt$$

triangle area formula:

$$\int_0^{T_s} i_L(t)\, dt = \frac{1}{2}\, i_{pk}\, (D_1 + D_2)T_s$$

$$\left\langle i_L \right\rangle = (V_g - V)\, \frac{D_1T_s}{2L}\, (D_1 + D_2)$$



equate dc component to dc load current:

$$\frac{V}{R} = \frac{D_1T_s}{2L}\, (D_1 + D_2)\, (V_g - V)$$

Solution for V

Two equations and two unknowns (V and D_2):

$$V = V_g \frac{D_1}{D_1 + D_2}$$ (from inductor volt-second balance)

$$\frac{V}{R} = \frac{D_1T_s}{2L}\, (D_1 + D_2)\, (V_g - V)$$ (from capacitor charge balance)

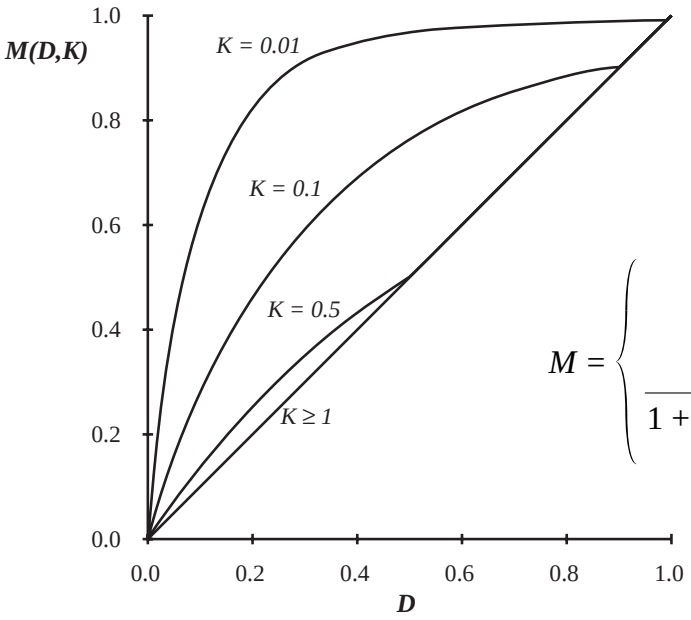
Eliminate D_2 , solve for V :

$$\frac{V}{V_g} = \frac{2}{1 + \sqrt{1 + 4K / D_1^2}}$$

where $K = 2L / RT_s$

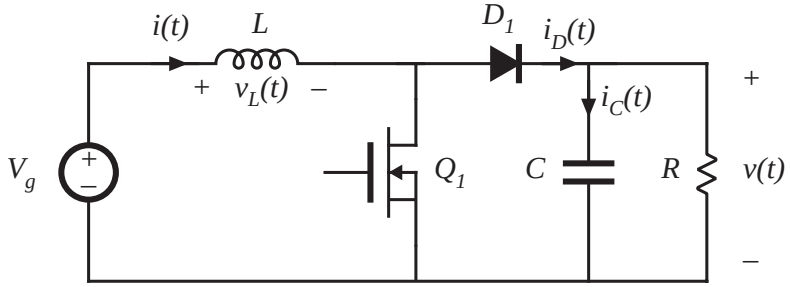
valid for $K < K_{crit}$

Buck converter *M(D,K)*



$$M = \begin{cases} D & \text{for } K > K_{crit} \\ \dfrac{2}{1 + \sqrt{1 + 4K / D^2}} & \text{for } K < K_{crit} \end{cases}$$

5.3. Boost converter example



Mode boundary:

$I > \Delta i_L$ *for CCM*

$I < \Delta i_L$ *for DCM*

Previous CCM soln:

$$I = \frac{V_g}{D'^2 R} \qquad \Delta i_L = \frac{V_g}{2L} DT_s$$

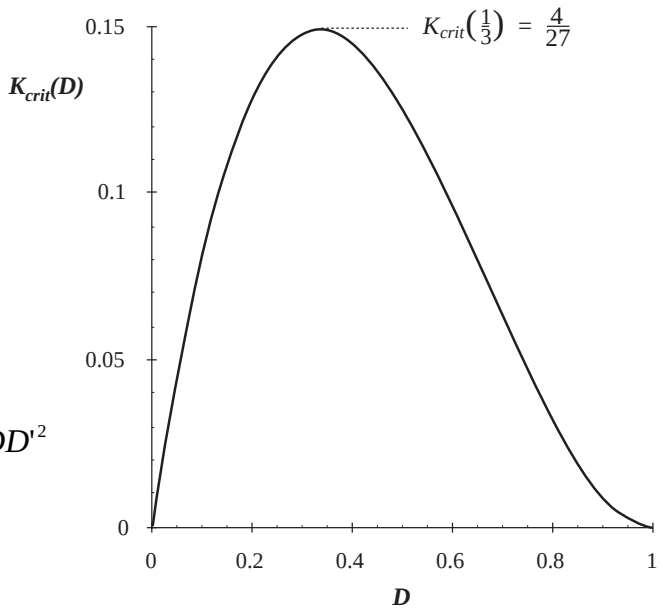
Mode boundary

$$\frac{V_g}{D'^2 R} > \frac{DT_s V_g}{2L} \qquad \text{for CCM}$$

$$\frac{2L}{RT_s} > DD'^2 \qquad \text{for CCM}$$

$$K > K_{crit}(D) \qquad \text{for CCM}$$
$$K < K_{crit}(D) \qquad \text{for DCM}$$

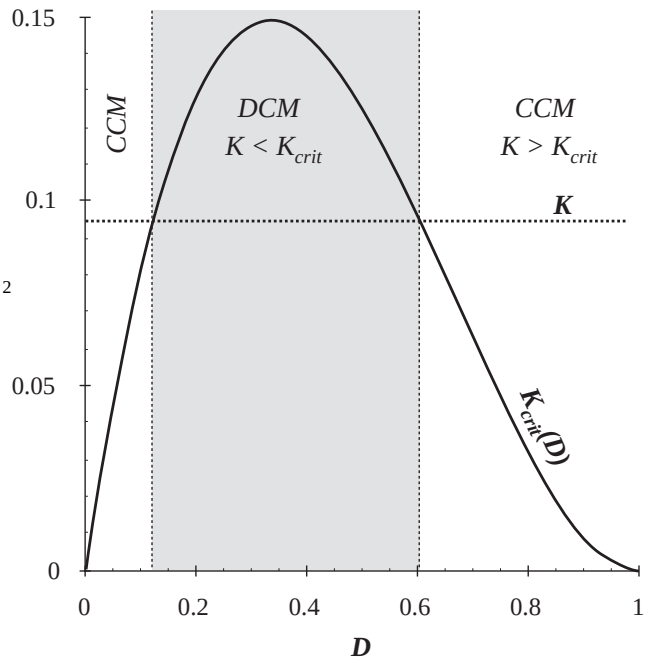
where $K = \frac{2L}{RT_s}$ and $K_{crit}(D) = DD'^2$



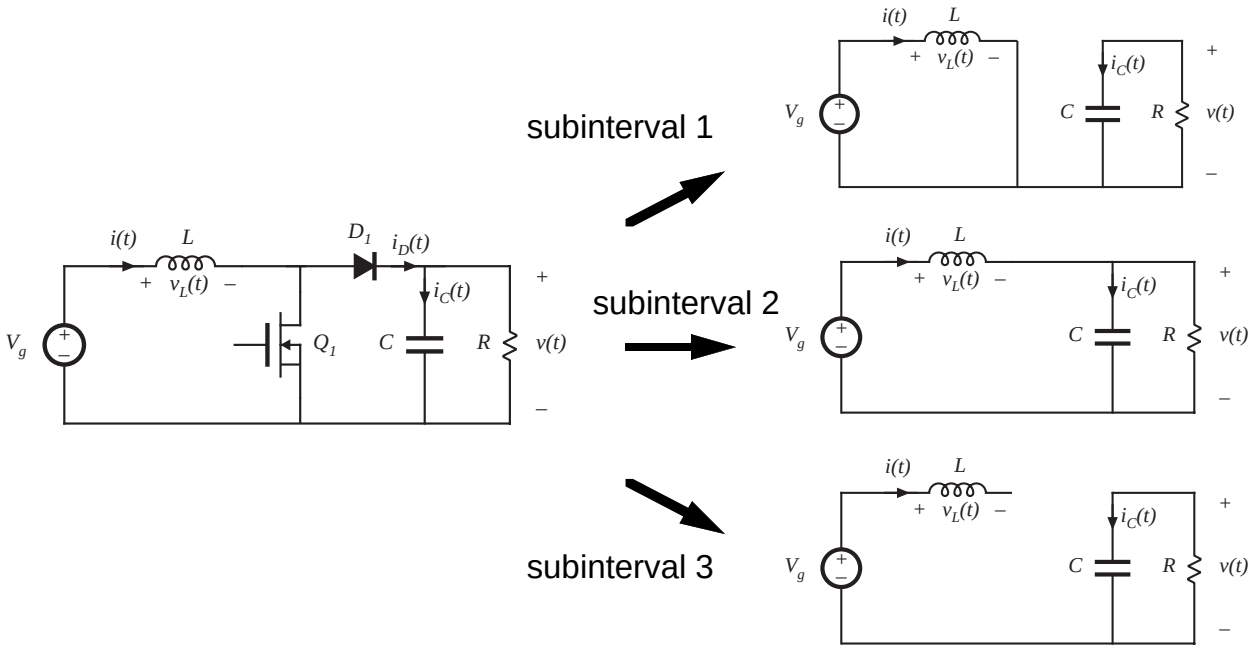
Mode boundary

$$K > K_{crit}(D) \qquad \text{for CCM}$$
$$K < K_{crit}(D) \qquad \text{for DCM}$$

where $K = \frac{2L}{RT_s}$ and $K_{crit}(D) = DD'^2$



Conversion ratio: DCM boost

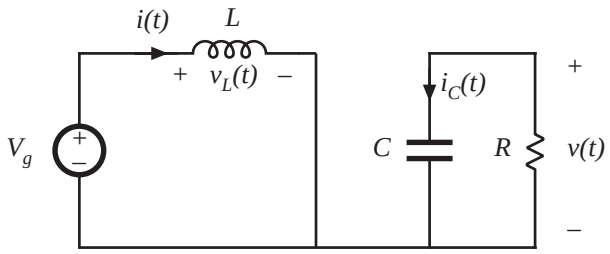


Subinterval 1

$$v_L(t) = V_g$$
$$i_C(t) = -\,v(t) / R$$

Small ripple approximation for *v(t)* (but not for *i(t)*!):

$$v_L(t) \approx V_g$$
$$i_C(t) \approx -\,V / R$$



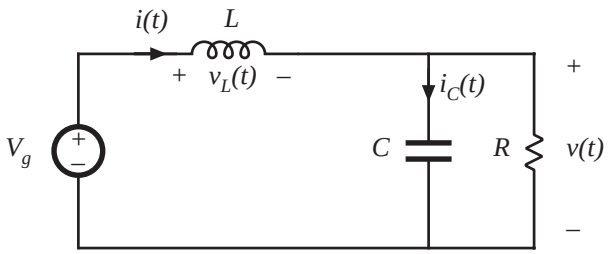
$$0 < t < D_1 T_s$$

Subinterval 2

$$v_L(t) = V_g - v(t)$$
$$i_C(t) = i(t) - v(t) / R$$

Small ripple approximation for *v(t)* but not for *i(t)*:

$$v_L(t) \approx V_g - V$$
$$i_C(t) \approx i(t) - V / R$$



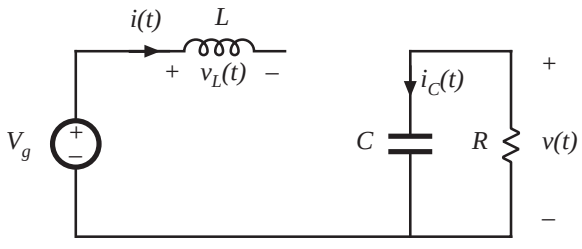
$$D_1 T_s < t < (D_1 + D_2) T_s$$

Subinterval 3

$$v_L = 0, \quad i = 0$$
$$i_C(t) = - v(t) / R$$

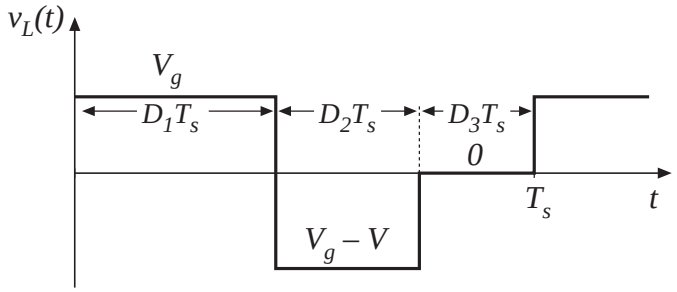
Small ripple approximation:

$$v_L(t) = 0$$
$$i_C(t) = - V / R$$



$$(D_1 + D_2) T_s < t < T_s$$

Inductor volt-second balance



Volt-second balance:

$$D_1 V_g + D_2(V_g - V) + D_3(0) = 0$$

Solve for V:

$$V = \frac{D_1 + D_2}{D_2} V_g$$

note that D_2 is unknown

Capacitor charge balance

node equation:

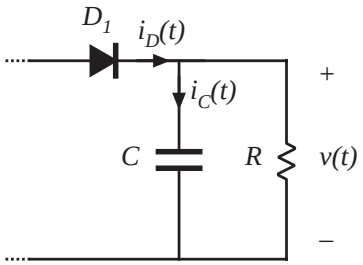
$$i_D(t) = i_C(t) + v(t) / R$$

capacitor charge balance:

$$\langle i_C \rangle = 0$$

hence

$$\langle i_D \rangle = V / R$$



must compute dc component of diode current and equate to load current (for this boost converter example)

Inductor and diode current waveforms

peak current:

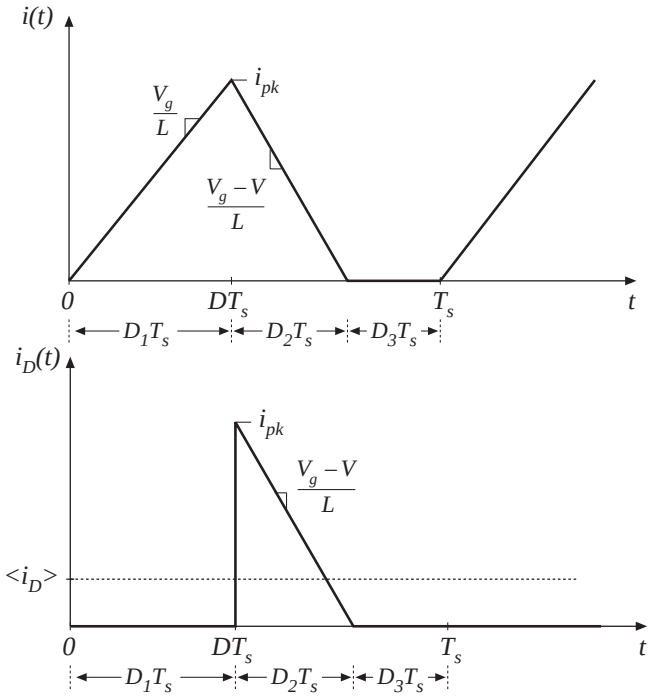
$$i_{pk} = \frac{V_g}{L} D_1 T_s$$

average diode current:

$$\left\langle i_D \right\rangle = \frac{1}{T_s} \int_0^{T_s} i_D(t)\, dt$$

triangle area formula:

$$\int_0^{T_s} i_D(t)\, dt = \frac{1}{2}\, i_{pk}\, D_2 T_s$$



Equate diode current to load current

average diode current:

$$\left\langle i_D \right\rangle = \frac{1}{T_s} \left(\frac{1}{2}\, i_{pk}\, D_2 T_s \right) = \frac{V_g D_1 D_2 T_s}{2L}$$

equate to dc load current:

$$\frac{V_g D_1 D_2 T_s}{2L} = \frac{V}{R}$$

Solution for V

Two equations and two unknowns (V and D_2):

$$V = \frac{D_1 + D_2}{D_2} V_g$$ (from inductor volt-second balance)

$$\frac{V_g D_1 D_2 T_s}{2L} = \frac{V}{R}$$ (from capacitor charge balance)

Eliminate D_2 , solve for V. From volt-sec balance eqn:

$$D_2 = D_1 \frac{V_g}{V - V_g}$$

Substitute into charge balance eqn, rearrange terms:

$$V^2 - VV_g - \frac{V_g^2 D_1^2}{K} = 0$$

Solution for V

$$V^2 - VV_g - \frac{V_g^2 D_1^2}{K} = 0$$

Use quadratic formula:

$$\frac{V}{V_g} = \frac{1 \pm \sqrt{1 + 4D_1^2 / K}}{2}$$

Note that one root leads to positive V, while other leads to negative V. Select positive root:

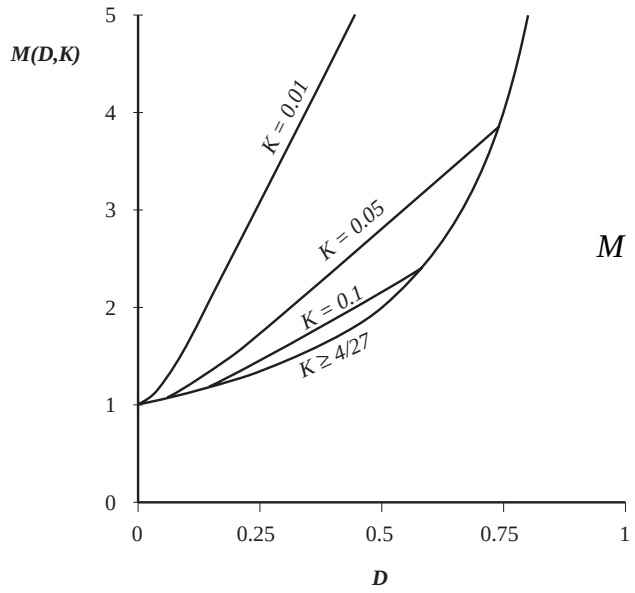
$$\frac{V}{V_g} = M(D_1, K) = \frac{1 + \sqrt{1 + 4D_1^2 / K}}{2}$$

where $K = 2L / RT_s$

valid for $K < K_{crit}(D)$

Transistor duty cycle D = interval *1* duty cycle D_1

Boost converter characteristics



$$M = \begin{cases} \dfrac{1}{1-D} & \text{for } K > K_{crit} \\ \dfrac{1+\sqrt{1+4D^2/K}}{2} & \text{for } K < K_{crit} \end{cases}$$

Approximate M in DCM:

$$M \approx \frac{1}{2} + \frac{D}{\sqrt{K}}$$

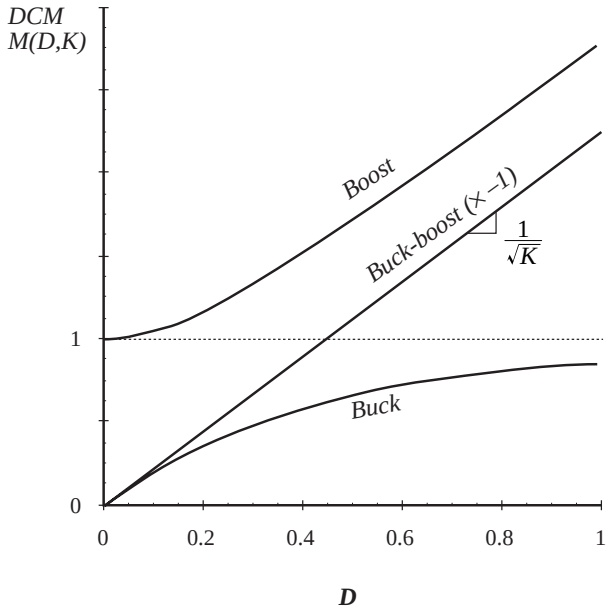
Summary of DCM characteristics

Table 5.2. Summary of CCM-DCM characteristics for the buck, boost, and buck-boost converters

Converter	$K_{crit}(D)$	*DCM* $M(D,K)$	*DCM* $D_2(D,K)$	*CCM* $M(D)$
Buck	$(1-D)$	$\dfrac{2}{1+\sqrt{1+4K/D^2}}$	$\dfrac{K}{D}M(D,K)$	D
Boost	$D(1-D)^2$	$\dfrac{1+\sqrt{1+4D^2/K}}{2}$	$\dfrac{K}{D}M(D,K)$	$\dfrac{1}{1-D}$
Buck-boost	$(1-D)^2$	$-\dfrac{D}{\sqrt{K}}$	$\sqrt{K}$	$-\dfrac{D}{1-D}$

with $K = 2L/RT_s$. *DCM occurs for* $K < K_{crit}$.

Summary of DCM characteristics



- DCM buck and boost characteristics are asymptotic to $M = 1$ and to the DCM buck-boost characteristic
- DCM buck-boost characteristic is linear
- CCM and DCM characteristics intersect at mode boundary. Actual M follows characteristic having larger magnitude
- DCM boost characteristic is nearly linear

Summary of key points

1. The discontinuous conduction mode occurs in converters containing current- or voltage-unidirectional switches, when the inductor current or capacitor voltage ripple is large enough to cause the switch current or voltage to reverse polarity.
2. Conditions for operation in the discontinuous conduction mode can be found by determining when the inductor current or capacitor voltage ripples and dc components cause the switch on-state current or off-state voltage to reverse polarity.
3. The dc conversion ratio M of converters operating in the discontinuous conduction mode can be found by application of the principles of inductor volt-second and capacitor charge balance.

Summary of key points

4. Extra care is required when applying the small-ripple approximation. Some waveforms, such as the output voltage, should have small ripple which can be neglected. Other waveforms, such as one or more inductor currents, may have large ripple that cannot be ignored.
5. The characteristics of a converter changes significantly when the converter enters DCM. The output voltage becomes load-dependent, resulting in an increase in the converter output impedance.

Chapter 6. Converter Circuits

6.1. Circuit manipulations

6.2. A short list of converters

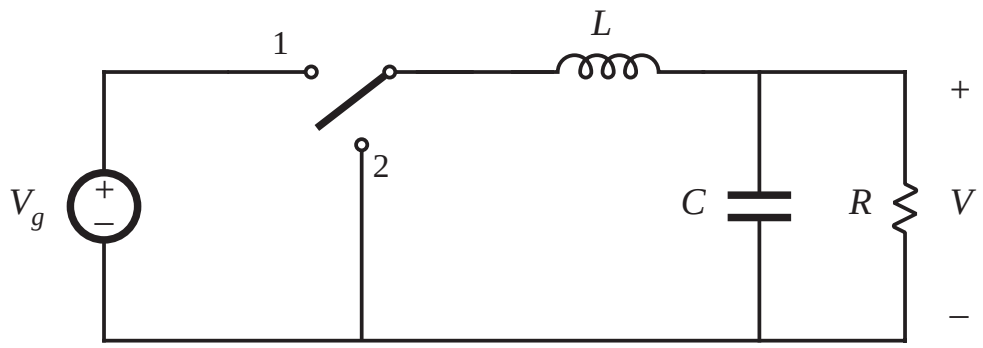
6.3. Transformer isolation

6.4. Converter evaluation and design

6.5. Summary of key points

- Where do the boost, buck-boost, and other converters originate?
- How can we obtain a converter having given desired properties?
- What converters are possible?
- How can we obtain transformer isolation in a converter?
- For a given application, which converter is best?

6.1. Circuit Manipulations



Begin with buck converter: derived in Chapter 1 from first principles

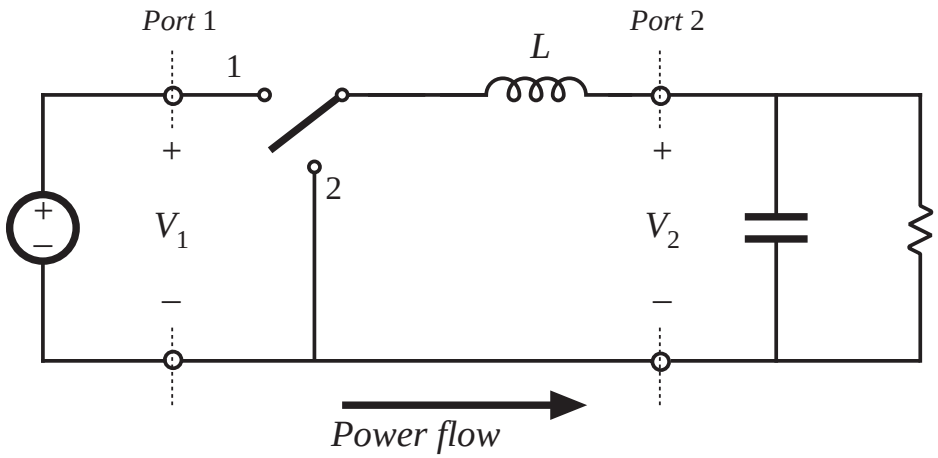
- Switch changes dc component, low-pass filter removes switching harmonics
- Conversion ratio is $M = D$

6.1.1. Inversion of source and load

Interchange power input and output ports of a converter

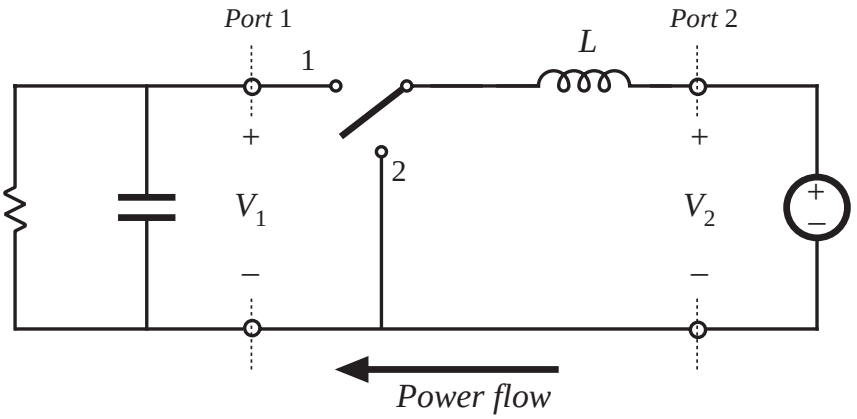
Buck converter example

$$V_2 = DV_1$$



Inversion of source and load

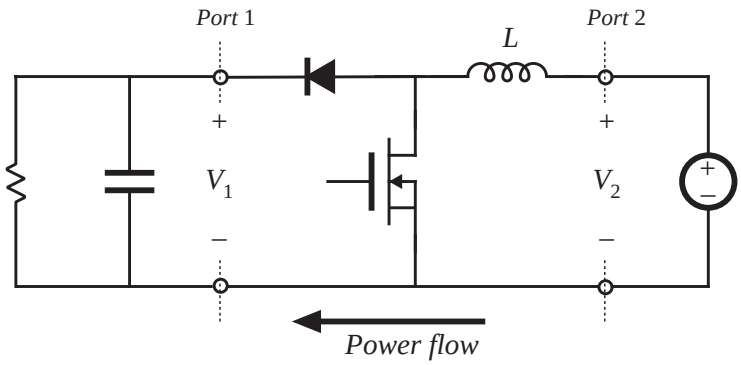
Interchange power source and load:



$$V_2 = DV_1 \qquad V_1 = \frac{1}{D} V_2$$

Realization of switches as in Chapter 4

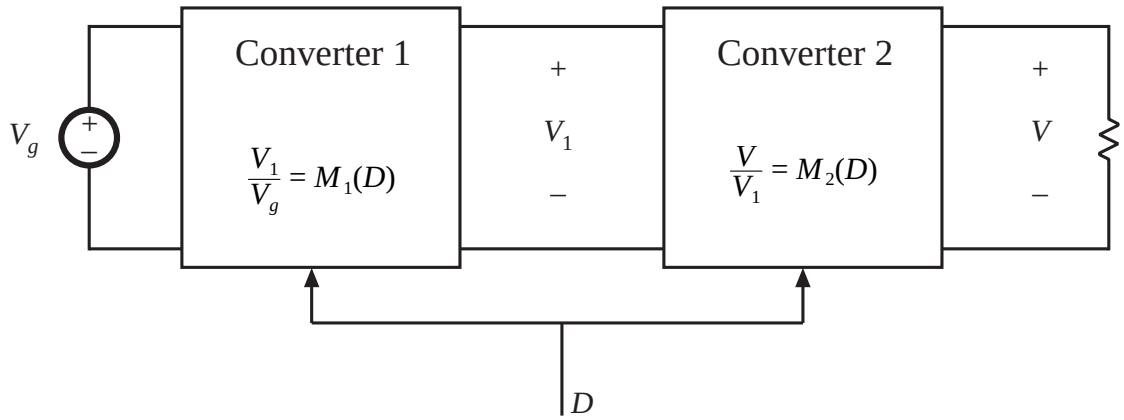
- Reversal of power flow requires new realization of switches
- Transistor conducts when switch is in position 2
- Interchange of D and D'



$$V_1 = \frac{1}{D'} V_2$$

Inversion of buck converter yields boost converter

6.1.2. Cascade connection of converters

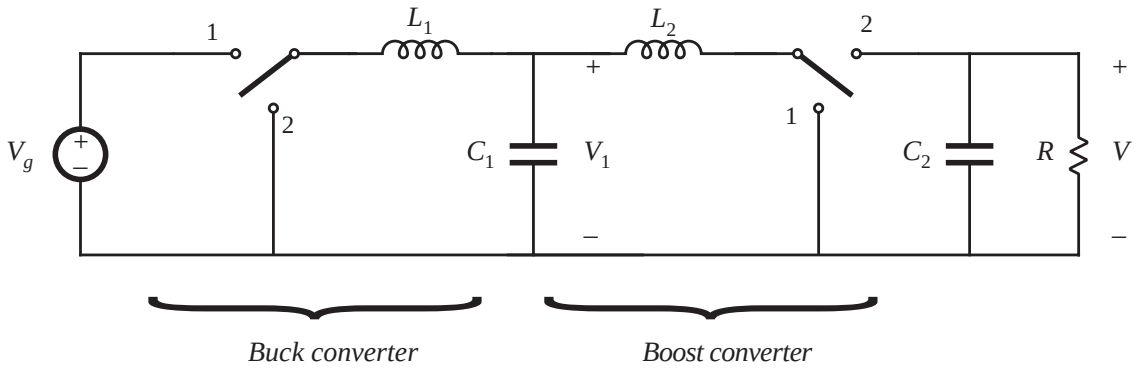


$$V_1 = M_1(D)V_g$$

$$V = M_2(D)V_1$$

$$\longrightarrow \quad \frac{V}{V_g} = M(D) = M_1(D)M_2(D)$$

Example: buck cascaded by boost



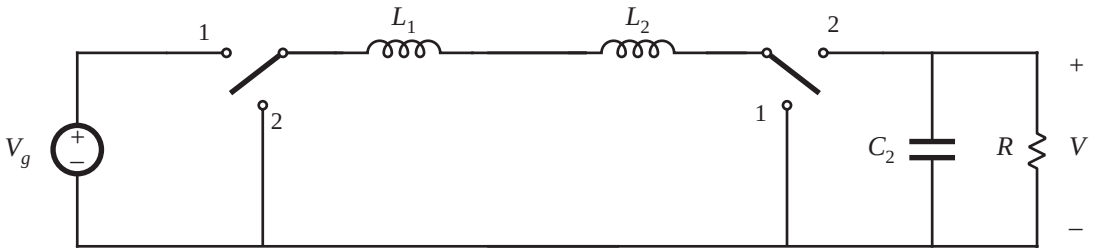
$$\frac{V_1}{V_g} = D$$

$$\frac{V}{V_1} = \frac{1}{1-D}$$

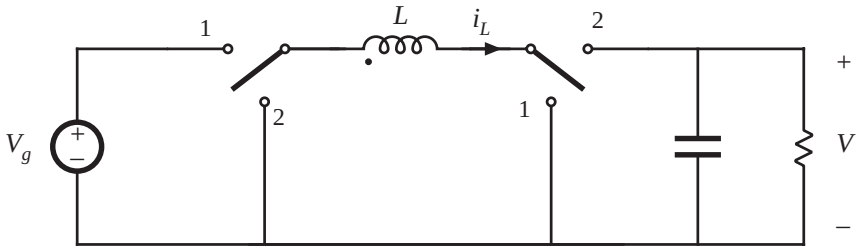
$$\longrightarrow \quad \frac{V}{V_g} = \frac{D}{1-D}$$

Buck cascaded by boost: simplification of internal filter

Remove capacitor C_1

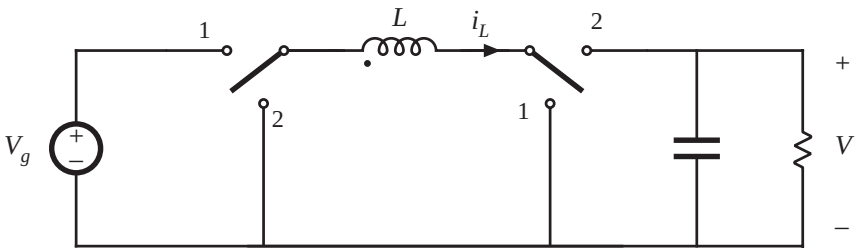


Combine inductors L_1 and L_2

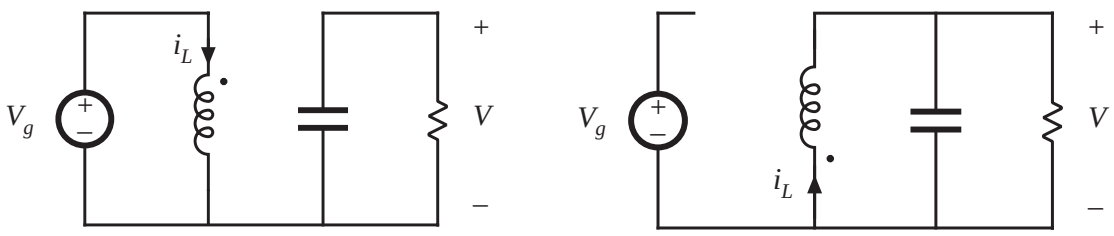


Noninverting buck-boost converter

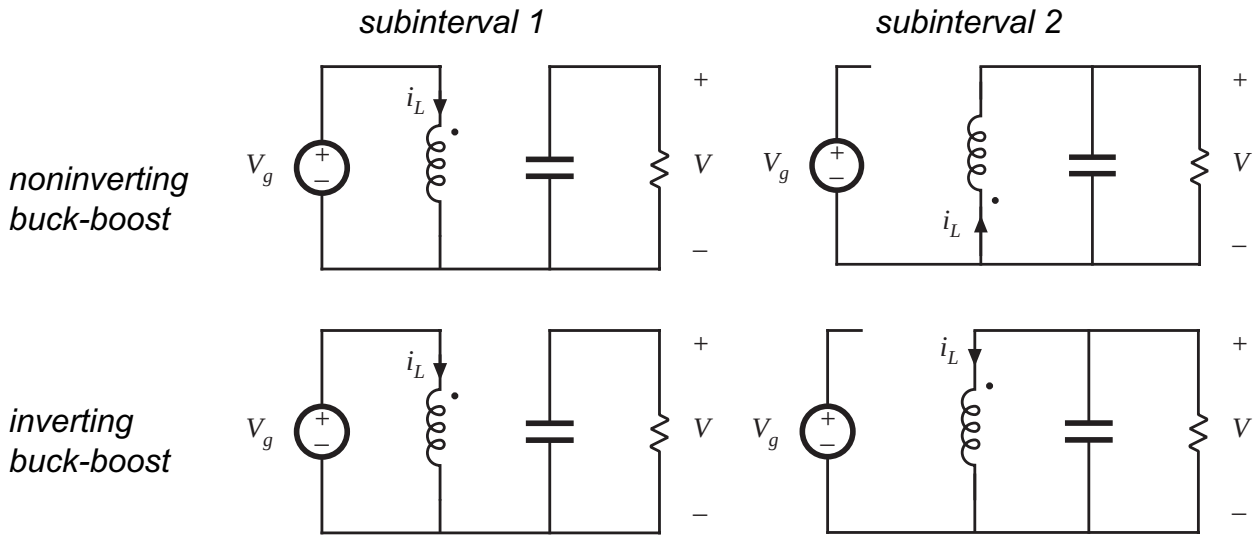
Noninverting buck-boost converter



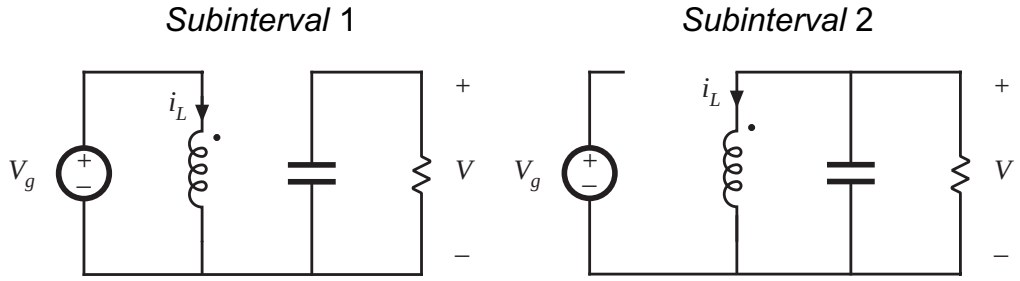
subinterval 1 *subinterval 2*



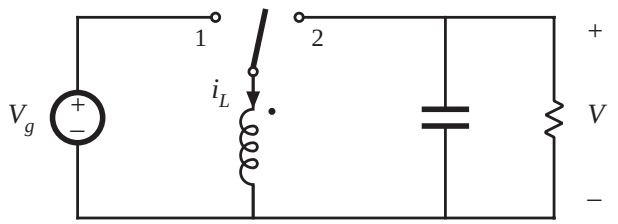
Reversal of output voltage polarity



Reduction of number of switches: inverting buck-boost



One side of inductor always connected to ground
— hence, only one SPDT switch needed:



$$\frac{V}{V_g} = -\frac{D}{1-D}$$

Discussion: cascade connections

- Properties of buck-boost converter follow from its derivation as buck cascaded by boost

  Equivalent circuit model: buck 1:D transformer cascaded by boost D':1 transformer

  Pulsating input current of buck converter

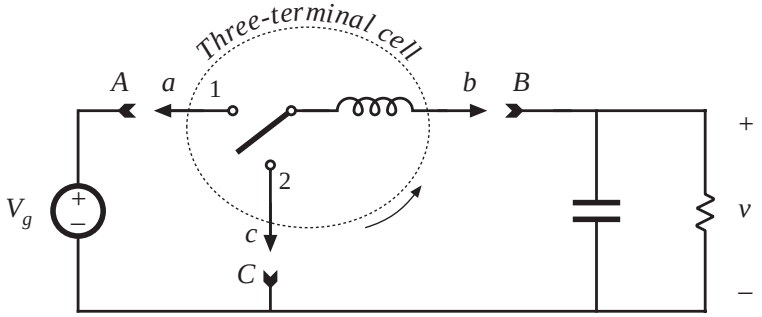
  Pulsating output current of boost converter

- Other cascade connections are possible

  Cuk converter: boost cascaded by buck

6.1.3. Rotation of three-terminal cell

Treat inductor and SPDT switch as three-terminal cell:

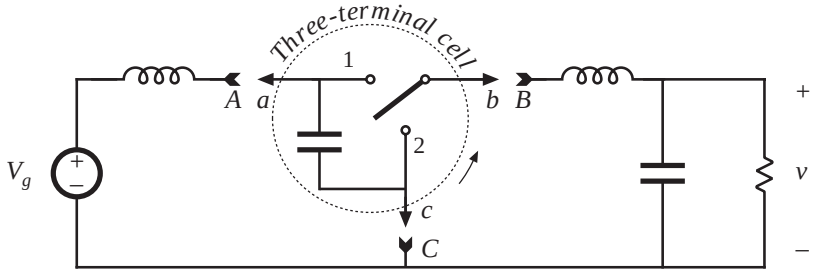


Three-terminal cell can be connected between source and load in three nontrivial distinct ways:

a-A b-B c-C	buck converter
a-C b-A c-B	boost converter
a-A b-C c-B	buck-boost converter

Rotation of a dual three-terminal network

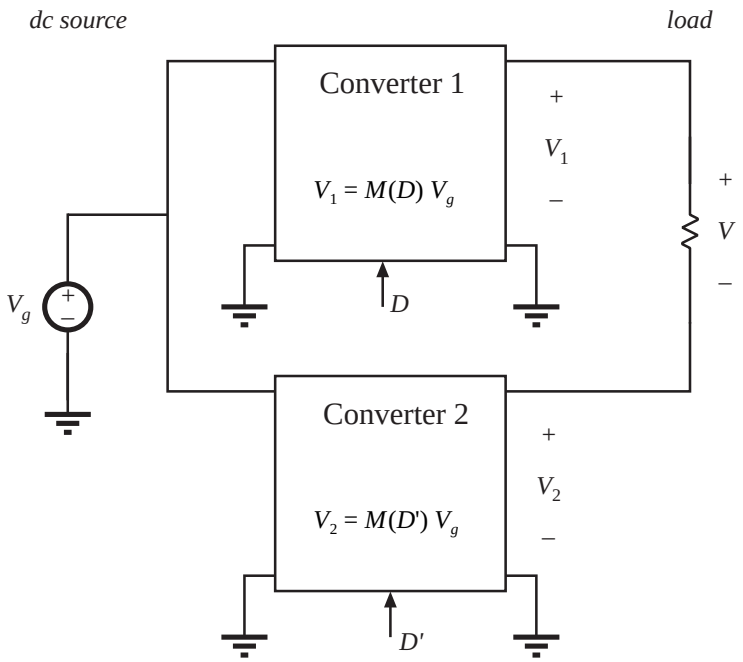
A capacitor and SPDT switch as a three-terminal cell:



Three-terminal cell can be connected between source and load in three nontrivial distinct ways:

a-A b-B c-C	buck converter with L-C input filter
a-C b-A c-B	boost converter with L-C output filter
a-A b-C c-B	Cuk converter

6.1.4. Differential connection of load to obtain bipolar output voltage

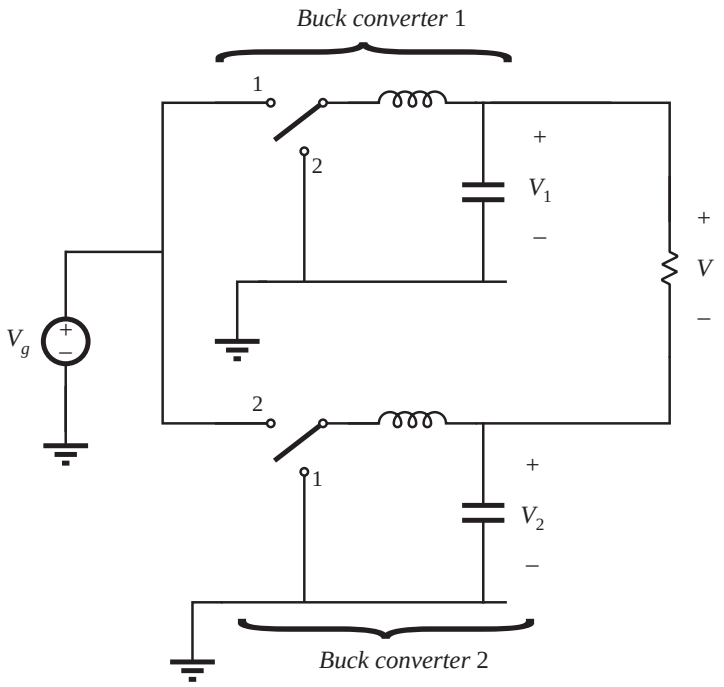


Differential load voltage is

$$V = V_1 - V_2$$

The outputs V_1 and V_2 may both be positive, but the differential output voltage V can be positive or negative.

Differential connection using two buck converters



Converter #1 transistor driven with duty cycle D

Converter #2 transistor driven with duty cycle complement D'

Differential load voltage is

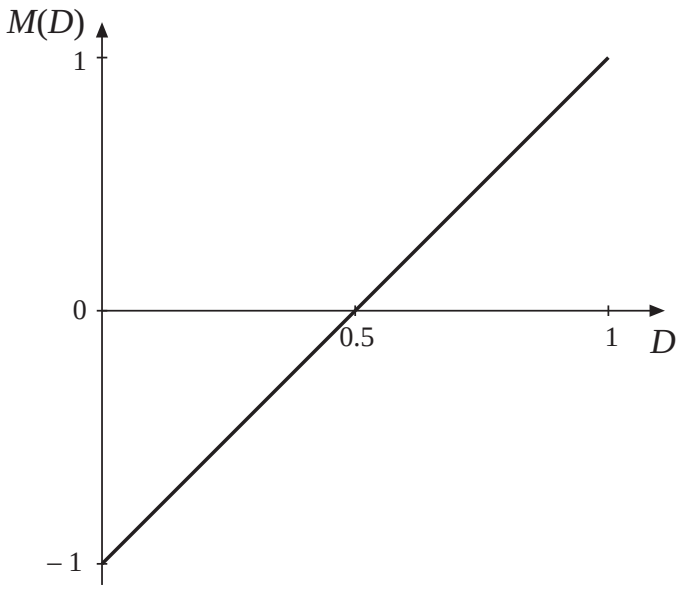
$$V = DV_g - D'V_g$$

Simplify:

$$V = (2D - 1)V_g$$

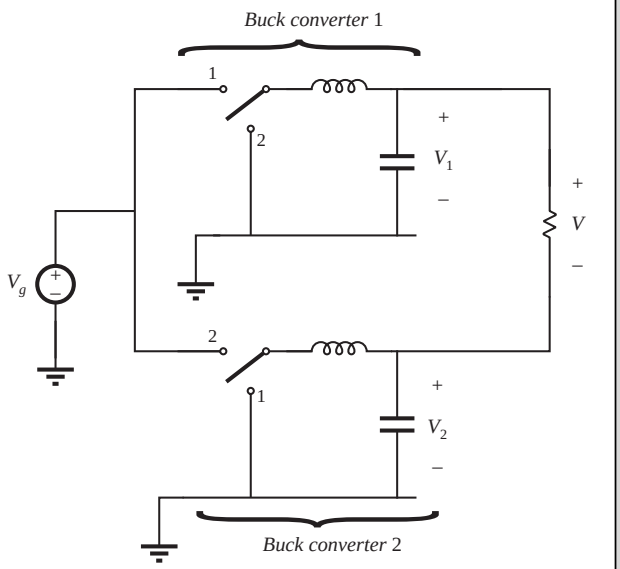
Conversion ratio $M(D)$, differentially-connected buck converters

$$V = (2D - 1)V_g$$

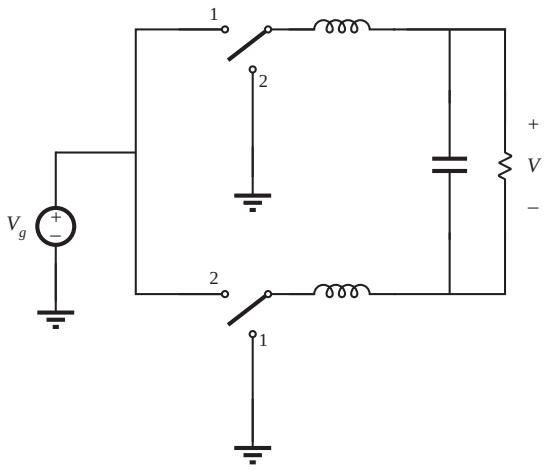


Simplification of filter circuit, differentially-connected buck converters

Original circuit

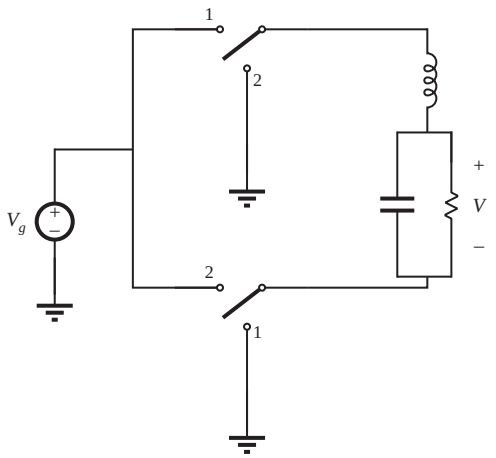


Bypass load directly with capacitor

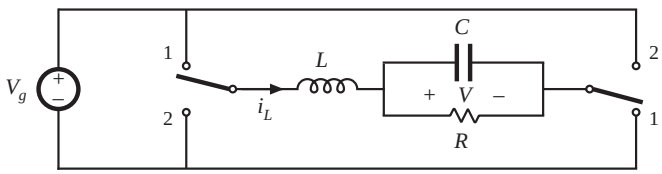


Simplification of filter circuit, differentially-connected buck converters

Combine series-connected inductors



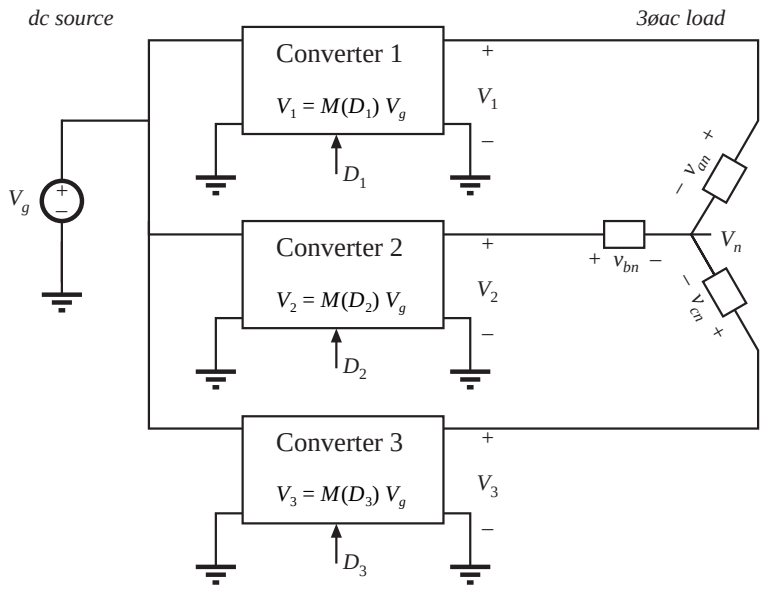
Re-draw for clarity



H-bridge, or bridge inverter

Commonly used in single-phase inverter applications and in servo amplifier applications

Differential connection to obtain 3ø inverter



With balanced 3ø load, neutral voltage is

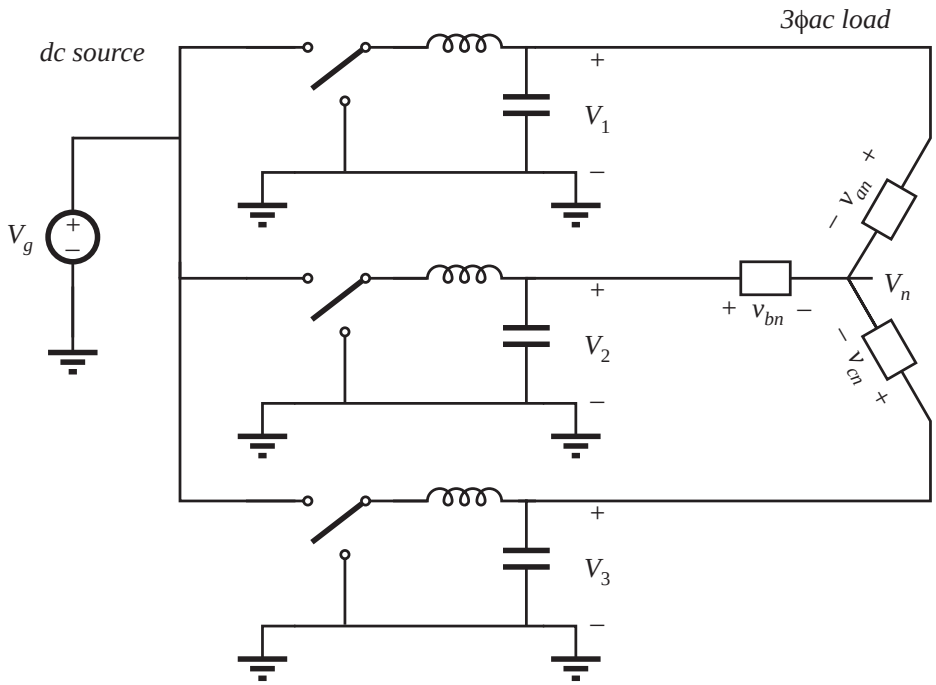
$$V_n = \frac{1}{3}\left(V_1 + V_2 + V_3\right)$$

Phase voltages are

$$V_{an} = V_1 - V_n$$
$$V_{bn} = V_2 - V_n$$
$$V_{cn} = V_3 - V_n$$

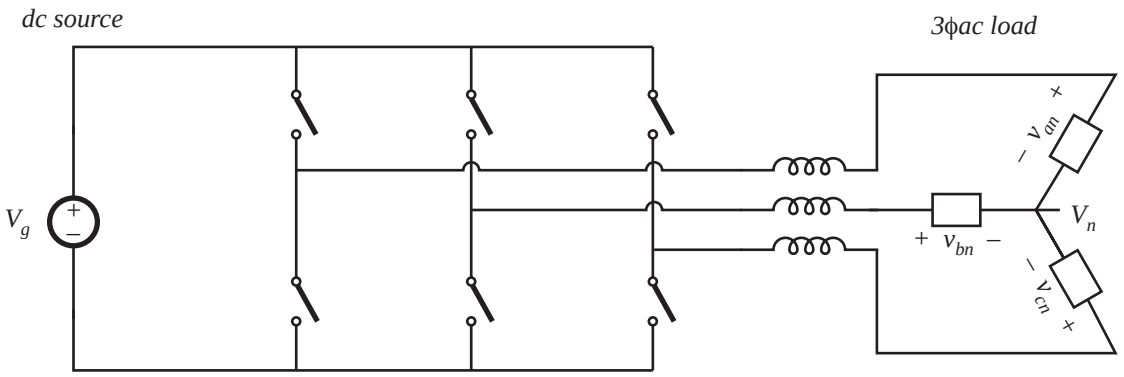
Control converters such that their output voltages contain the same dc biases. This dc bias will appear at the neutral point V_n. It then cancels out, so phase voltages contain no dc bias.

3ø differential connection of three buck converters



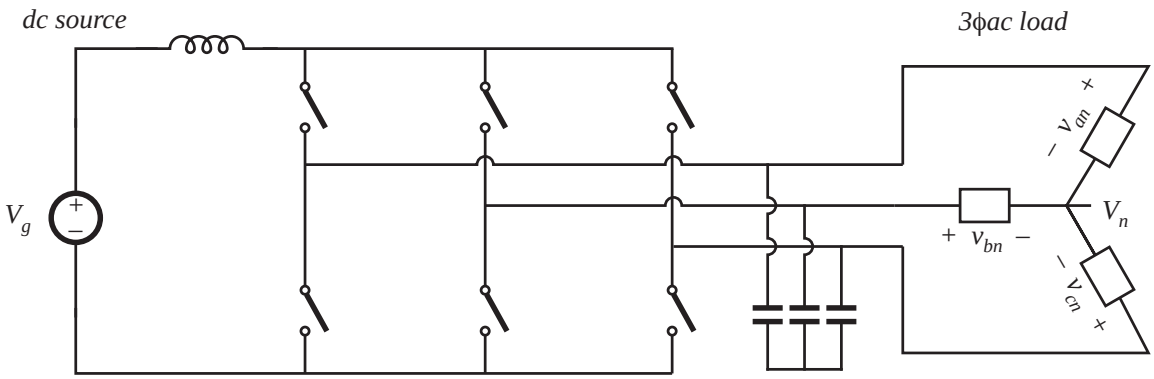
3ø differential connection of three buck converters

Re-draw for clarity:



"Voltage-source inverter" or buck-derived three-phase inverter

The 3ø current-source inverter



- Exhibits a boost-type conversion characteristic

6.2. A short list of converters

An infinite number of converters are possible, which contain switches embedded in a network of inductors and capacitors

Two simple classes of converters are listed here:

- Single-input single-output converters containing a single inductor. The switching period is divided into two subintervals. This class contains eight converters.
- Single-input single-output converters containing two inductors. The switching period is divided into two subintervals. Several of the more interesting members of this class are listed.

Single-input single-output converters containing one inductor

- Use switches to connect inductor between source and load, in one manner during first subinterval and in another during second subinterval
- There are a limited number of ways to do this, so all possible combinations can be found
- After elimination of degenerate and redundant cases, eight converters are found:

dc-dc converters

buck boost buck-boost noninverting buck-boost

dc-ac converters

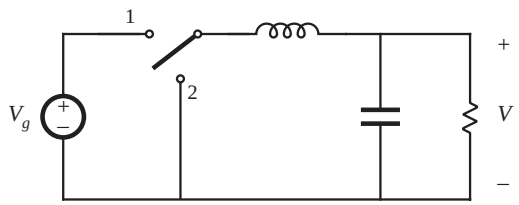
bridge Watkins-Johnson

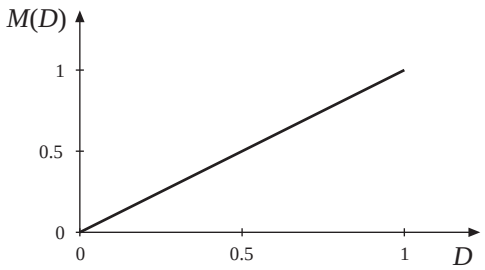
ac-dc converters

current-fed bridge inverse of Watkins-Johnson

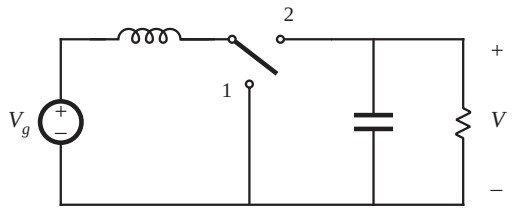
Converters producing a unipolar output voltage

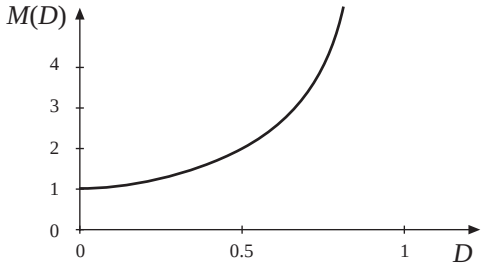
1. *Buck* $M(D) = D$





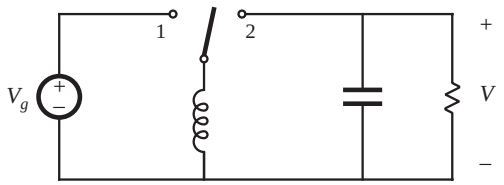
2. *Boost* $M(D) = \frac{1}{1-D}$

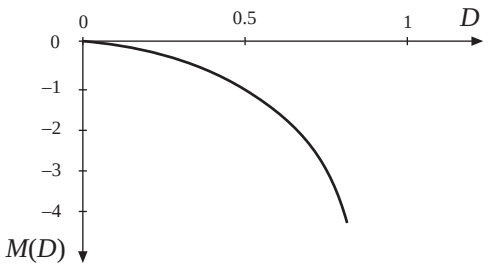




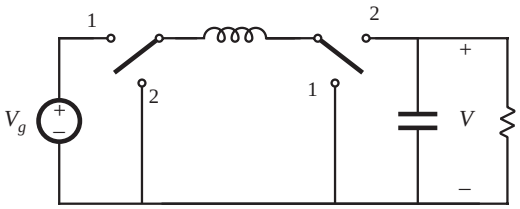
Converters producing a unipolar output voltage

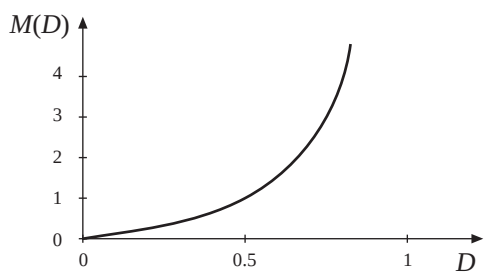
3. *Buck-boost* $M(D) = -\frac{D}{1-D}$





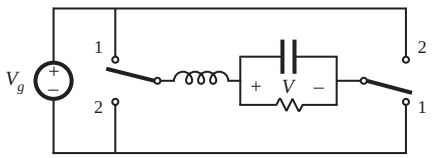
4. *Noninverting buck-boost* $M(D) = \frac{D}{1-D}$

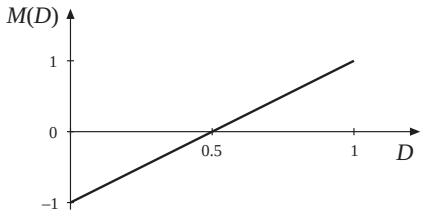




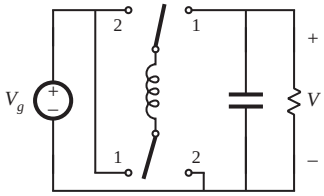
Converters producing a bipolar output voltage suitable as dc-ac inverters

5. *Bridge* $M(D) = 2D - 1$

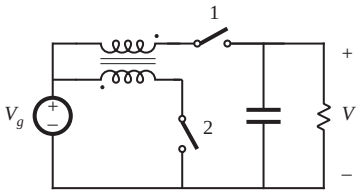


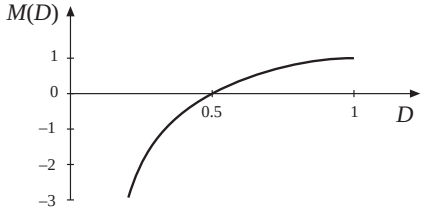


6. *Watkins-Johnson* $M(D) = \frac{2D-1}{D}$



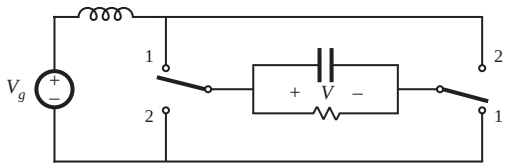
or

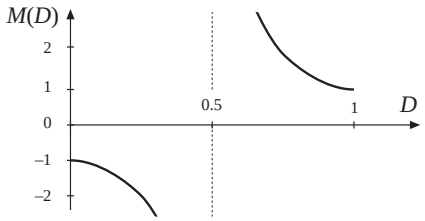




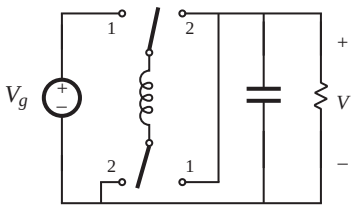
Converters producing a bipolar output voltage suitable as ac-dc rectifiers

7. *Current-fed bridge* $M(D) = \frac{1}{2D-1}$

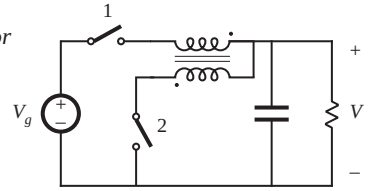


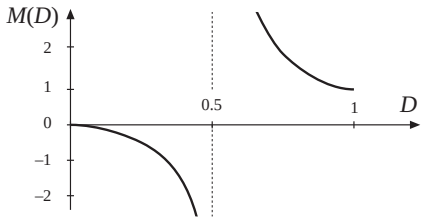


8. *Inverse of Watkins-Johnson* $M(D) = \frac{D}{2D-1}$



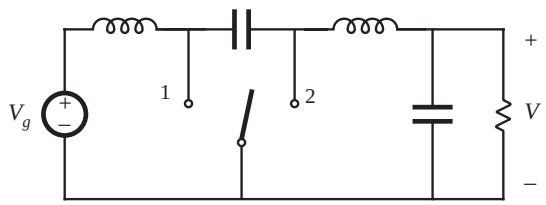
or

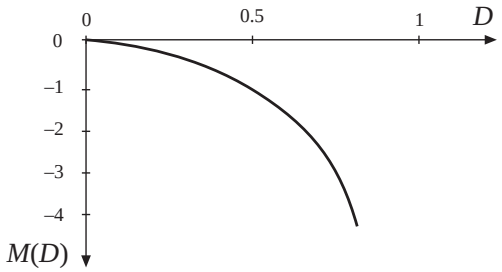




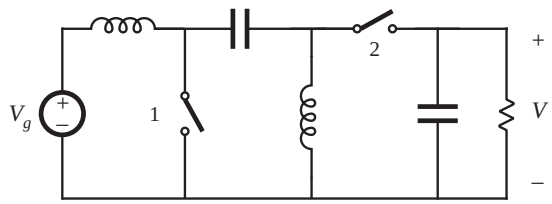
Several members of the class of two-inductor converters

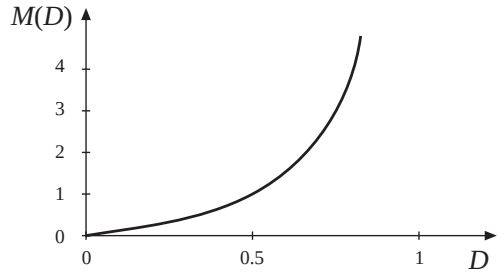
1. *Ćuk* $M(D) = -\frac{D}{1-D}$





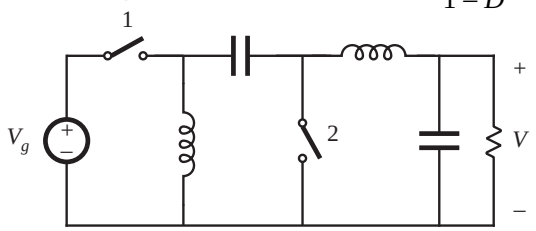
2. *SEPIC* $M(D) = \frac{D}{1-D}$

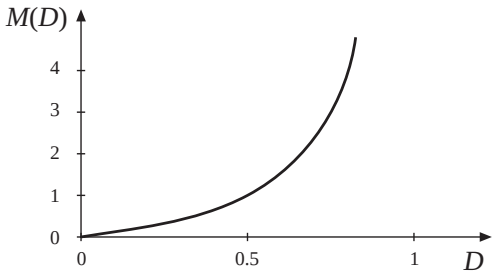




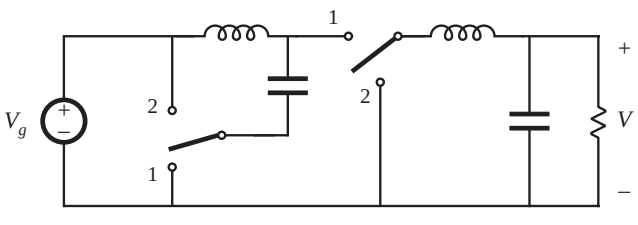
Several members of the class of two-inductor converters

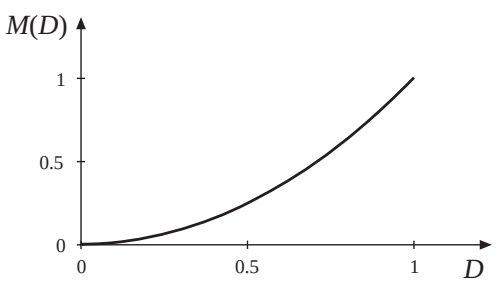
3. *Inverse of SEPIC* $M(D) = \frac{D}{1-D}$





4. *Buck* [2] $M(D) = D^2$





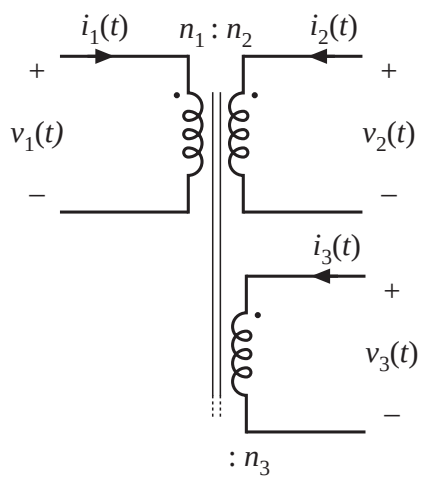
6.3. Transformer isolation

Objectives:

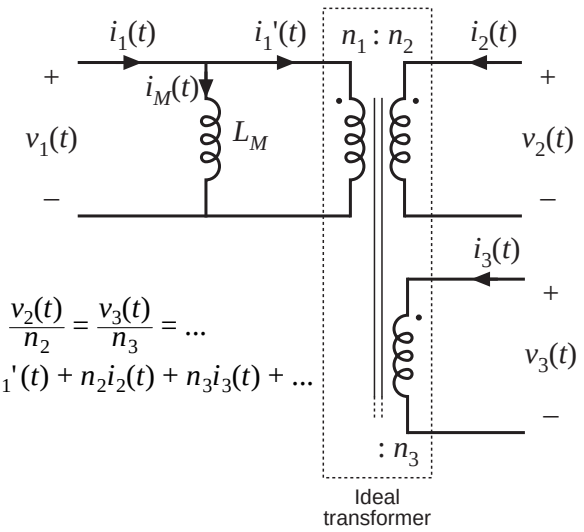
- Isolation of input and output ground connections, to meet safety requirements
- Reduction of transformer size by incorporating high frequency isolation transformer inside converter
- Minimization of current and voltage stresses when a large step-up or step-down conversion ratio is needed —use transformer turns ratio
- Obtain multiple output voltages via multiple transformer secondary windings and multiple converter secondary circuits

A simple transformer model

Multiple winding transformer



Equivalent circuit model

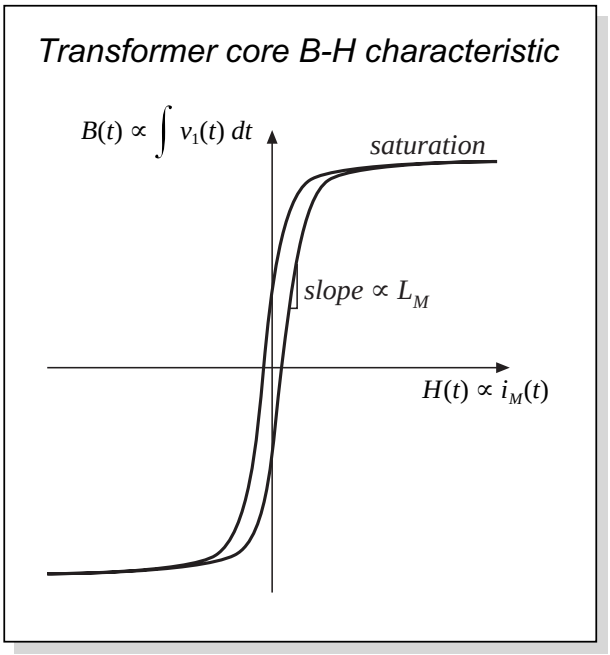


$$\frac{v_1(t)}{n_1} = \frac{v_2(t)}{n_2} = \frac{v_3(t)}{n_3} = \ldots$$

$$0 = n_1 i_1'(t) + n_2 i_2(t) + n_3 i_3(t) + \ldots$$

The magnetizing inductance L_M

- Models magnetization of transformer core material
- Appears effectively in parallel with windings
- If all secondary windings are disconnected, then primary winding behaves as an inductor, equal to the magnetizing inductance
- At dc: magnetizing inductance tends to short-circuit. Transformers cannot pass dc voltages
- Transformer saturates when magnetizing current i_M is too large



Volt-second balance in L_M

The magnetizing inductance is a real inductor, obeying

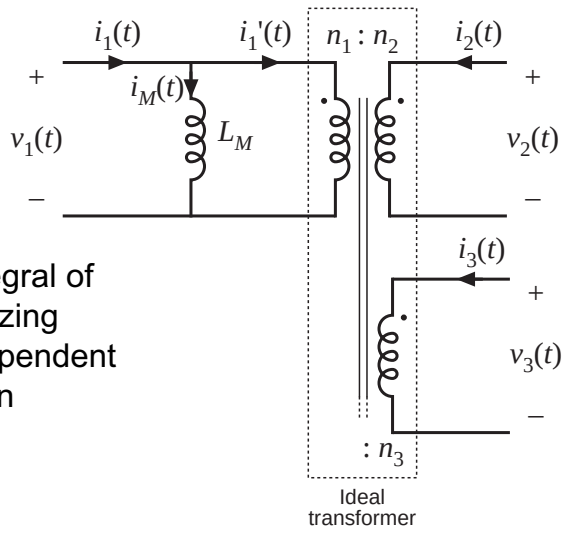
$$v_1(t) = L_M \frac{di_M(t)}{dt}$$

integrate:

$$i_M(t) - i_M(0) = \frac{1}{L_M} \int_0^t v_1(\tau) d\tau$$

Magnetizing current is determined by integral of the applied winding voltage. The magnetizing current and the winding currents are independent quantities. Volt-second balance applies: in steady-state, $i_M(T_s) = i_M(0)$, and hence

$$0 = \frac{1}{T_s} \int_0^{T_s} v_1(t) dt$$

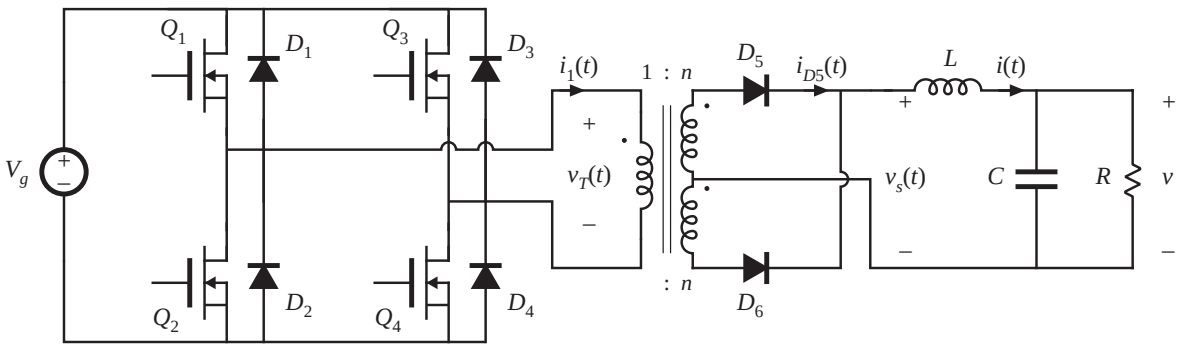


Transformer reset

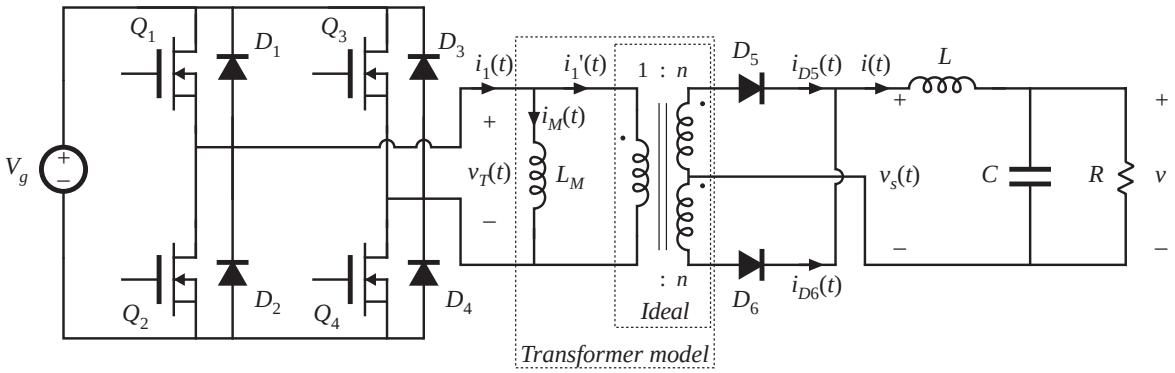
- "Transformer reset" is the mechanism by which magnetizing inductance volt-second balance is obtained
- The need to reset the transformer volt-seconds to zero by the end of each switching period adds considerable complexity to converters
- To understand operation of transformer-isolated converters:
  - replace transformer by equivalent circuit model containing magnetizing inductance
  - analyze converter as usual, treating magnetizing inductance as any other inductor
  - apply volt-second balance to all converter inductors, including magnetizing inductance

6.3.1. Full-bridge and half-bridge isolated buck converters

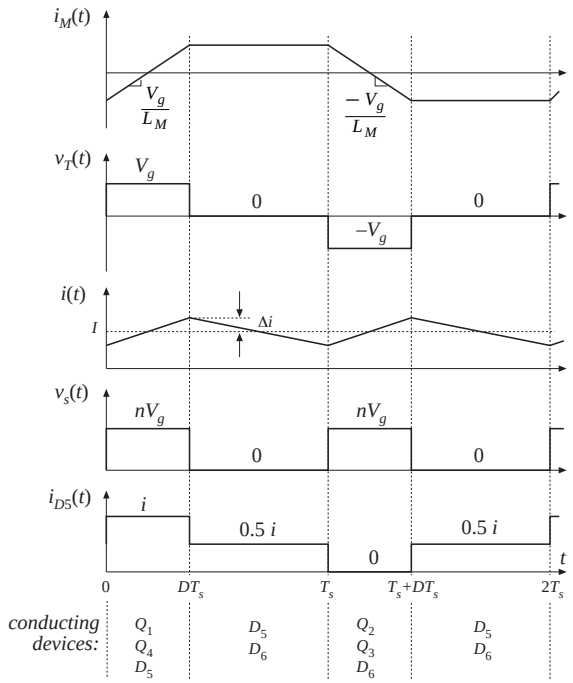
Full-bridge isolated buck converter



Full-bridge, with transformer equivalent circuit



Full-bridge: waveforms



- During first switching period: transistors Q_1 and Q_4 conduct for time DT_s , applying volt-seconds $V_g\,DT_s$ to primary winding
- During next switching period: transistors Q_2 and Q_3 conduct for time DT_s , applying volt-seconds $-V_g\,DT_s$ to primary winding
- Transformer volt-second balance is obtained over two switching periods
- Effect of nonidealities?

Effect of nonidealities on transformer volt-second balance

Volt-seconds applied to primary winding during first switching period:

$$(V_g - (Q_1 \text{ and } Q_4 \text{ forward voltage drops}))(Q_1 \text{ and } Q_4 \text{ conduction time})$$

Volt-seconds applied to primary winding during next switching period:

$$-(V_g - (Q_2 \text{ and } Q_3 \text{ forward voltage drops}))(Q_2 \text{ and } Q_3 \text{ conduction time})$$

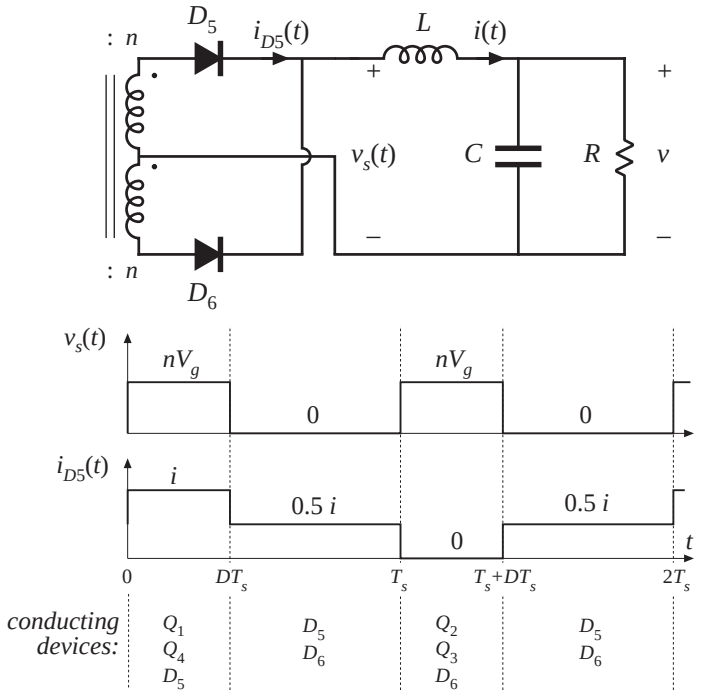
These volt-seconds never add to *exactly* zero.

Net volt-seconds are applied to primary winding

Magnetizing current slowly increases in magnitude

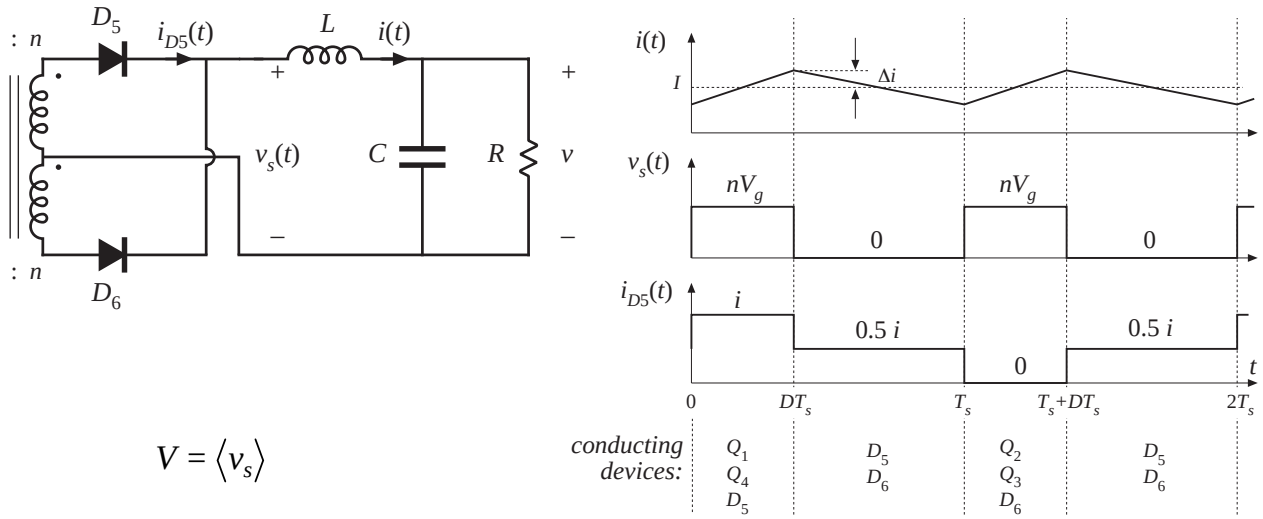
Saturation can be prevented by placing a capacitor in series with primary, or by use of current programmed mode (Chapter 12)

Operation of secondary-side diodes



- During second (D') subinterval, both secondary-side diodes conduct
- Output filter inductor current divides approximately equally between diodes
- Secondary amp-turns add to approximately zero
- Essentially no net magnetization of transformer core by secondary winding currents

Volt-second balance on output filter inductor

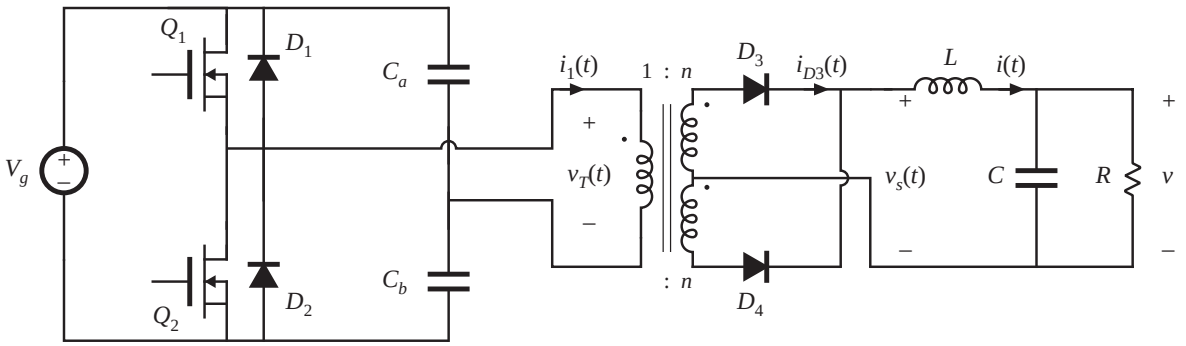


$$V = \langle v_s \rangle$$

$$V = nDV_g$$

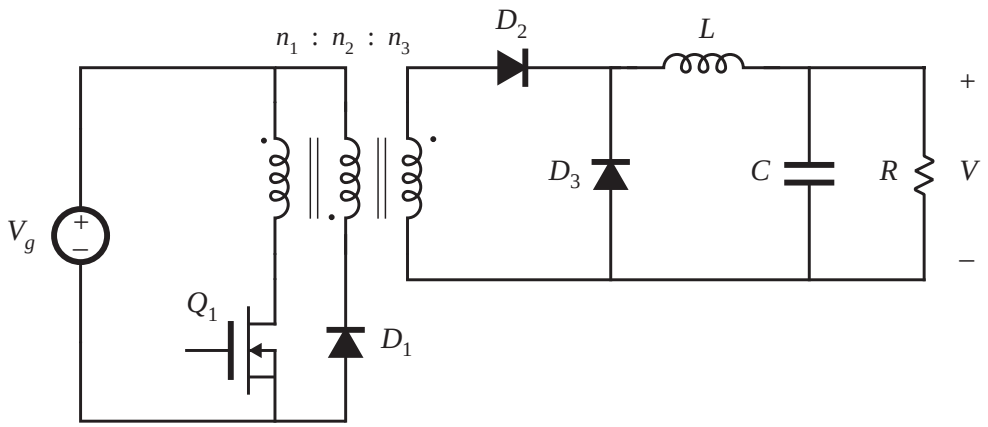
$M(D) = nD$ buck converter with turns ratio

Half-bridge isolated buck converter



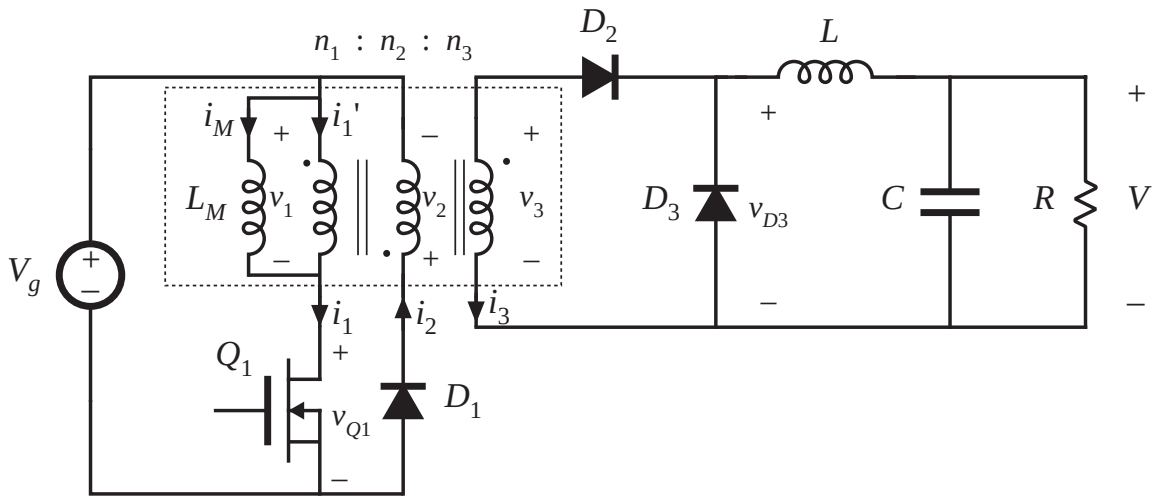
- Replace transistors Q_3 and Q_4 with large capacitors
- Voltage at capacitor centerpoint is $0.5V_g$
- $v_s(t)$ is reduced by a factor of two
- $M = 0.5\ nD$

6.3.2. Forward converter

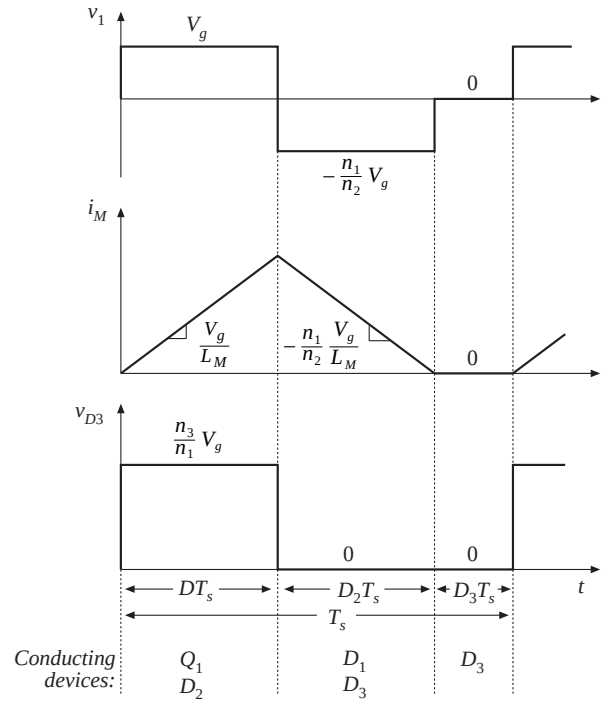


- Buck-derived transformer-isolated converter
- Single-transistor and two-transistor versions
- Maximum duty cycle is limited
- Transformer is reset while transistor is off

Forward converter with transformer equivalent circuit

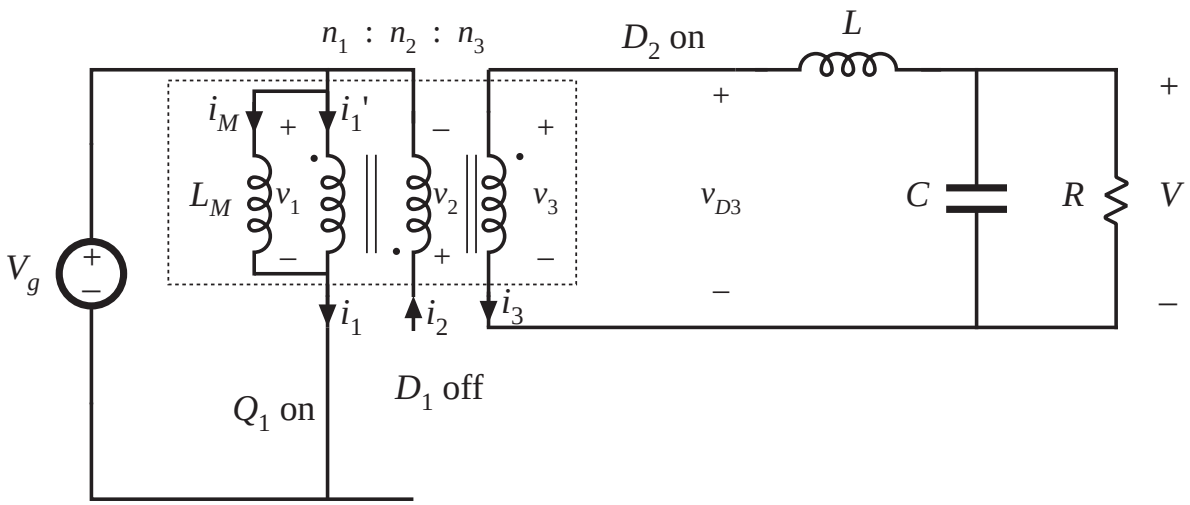


Forward converter: waveforms

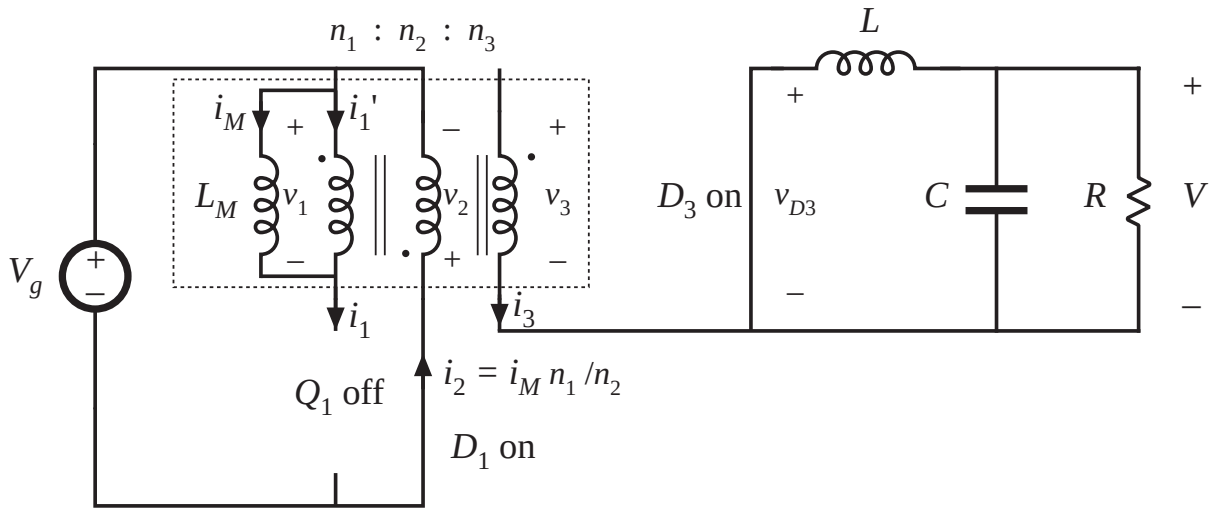


- Magnetizing current, in conjunction with diode D_1, operates in discontinuous conduction mode
- Output filter inductor, in conjunction with diode D_3, may operate in either CCM or DCM

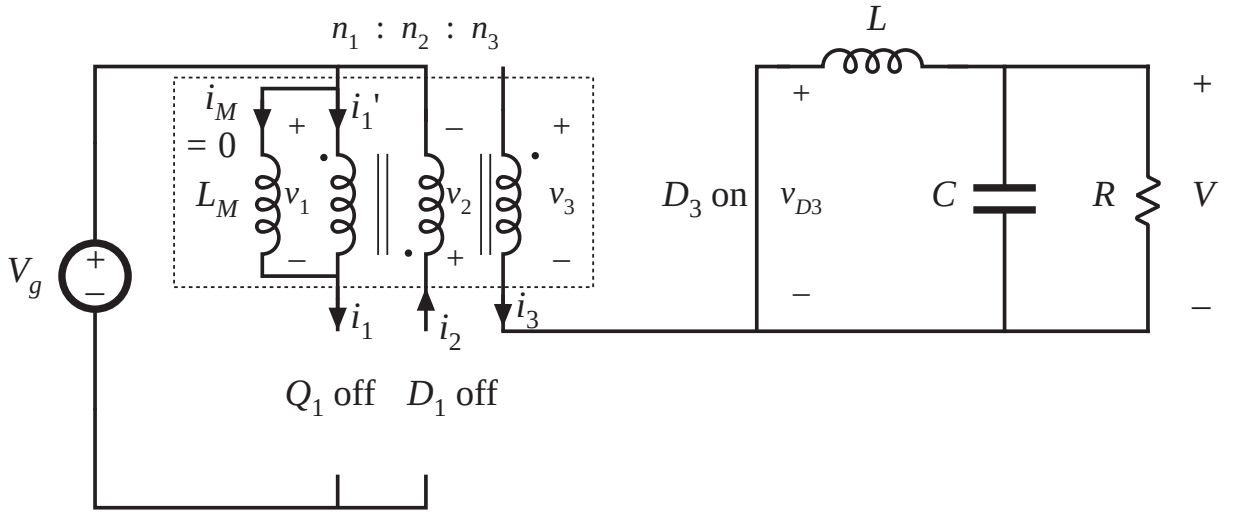
Subinterval 1: transistor conducts



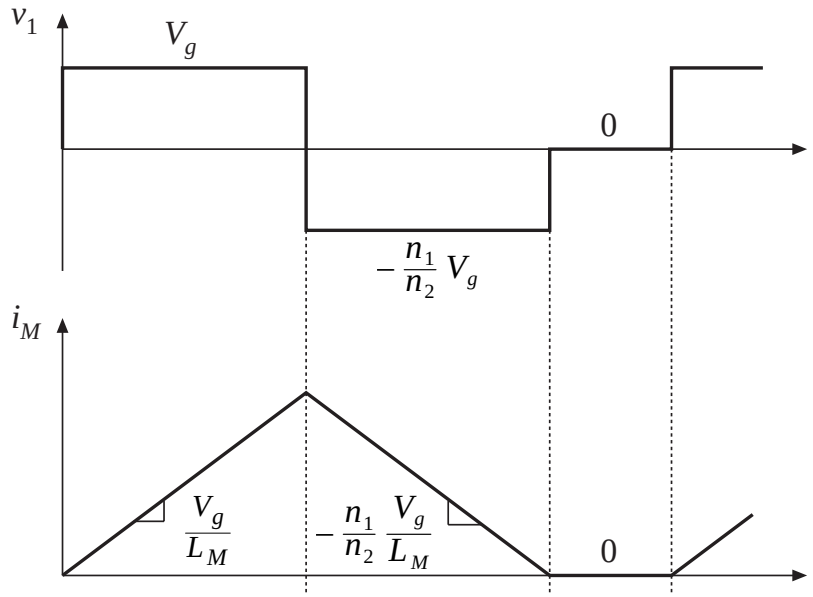
Subinterval 2: transformer reset



Subinterval 3



Magnetizing inductance volt-second balance



$$\langle v_1 \rangle = D\left(V_g\right) + D_2\left(-V_g n_1/n_2\right) + D_3\left(0\right) = 0$$

Transformer reset

From magnetizing current volt-second balance:

$$\langle v_1 \rangle = D\left(V_g\right) + D_2\left(-V_g n_1/n_2\right) + D_3\left(0\right) = 0$$

Solve for D_2:

$$D_2 = \frac{n_2}{n_1} D$$

D_3 cannot be negative. But $D_3 = 1 - D - D_2$. Hence

$$D_3 = 1 - D - D_2 \geq 0$$

$$D_3 = 1 - D\left(1 + \frac{n_2}{n_1}\right) \geq 0$$

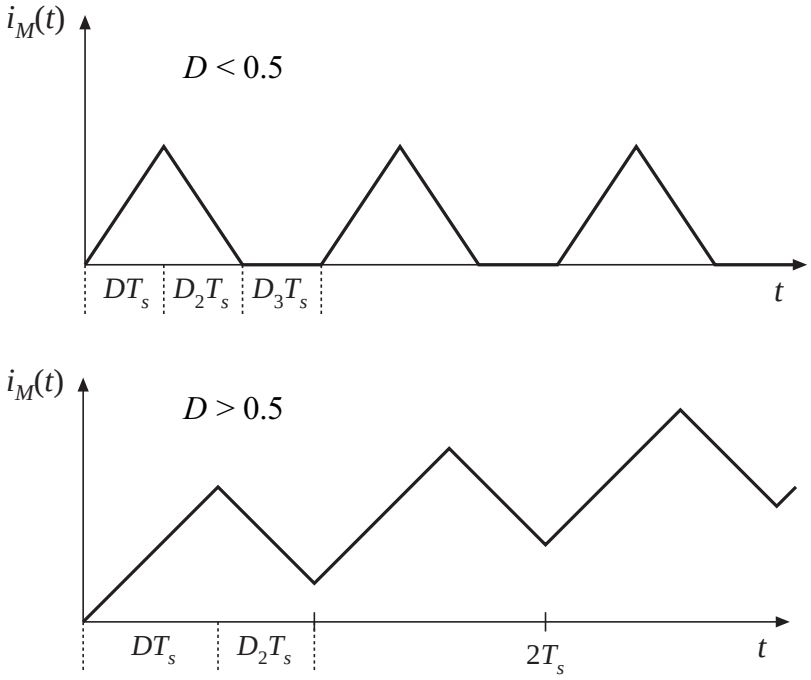
Solve for D

$$D \leq \frac{1}{1 + \frac{n_2}{n_1}}$$

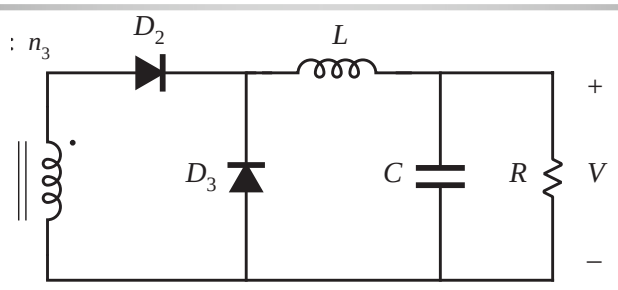
for $n_1 = n_2$: $D \leq \frac{1}{2}$

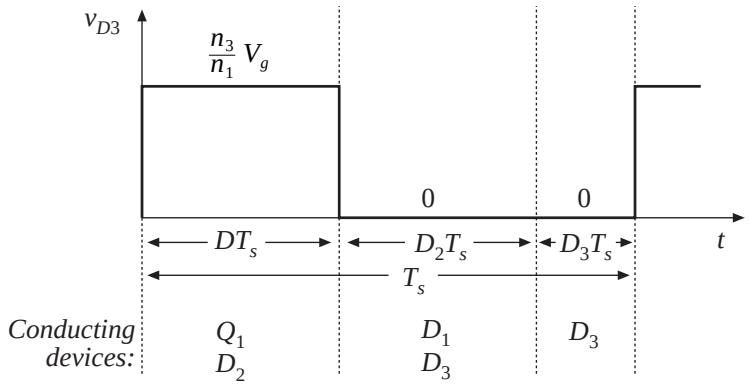
What happens when $D > 0.5$

magnetizing current waveforms, for $n_1 = n_2$



Conversion ratio *M(D)*





$$\langle v_{D3} \rangle = V = \frac{n_3}{n_1} DV_g$$

Maximum duty cycle vs. transistor voltage stress

Maximum duty cycle limited to

$$D \le \frac{1}{1 + \frac{n_2}{n_1}}$$

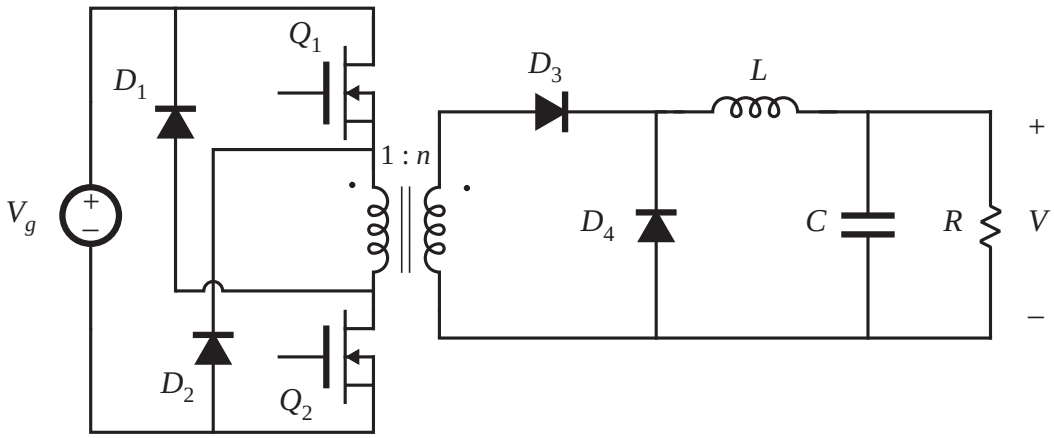
which can be increased by decreasing the turns ratio n_2 / n_1. But this increases the peak transistor voltage:

$$\max\left(v_{Q1}\right) = V_g\left(1 + \frac{n_1}{n_2}\right)$$

For $n_1 = n_2$

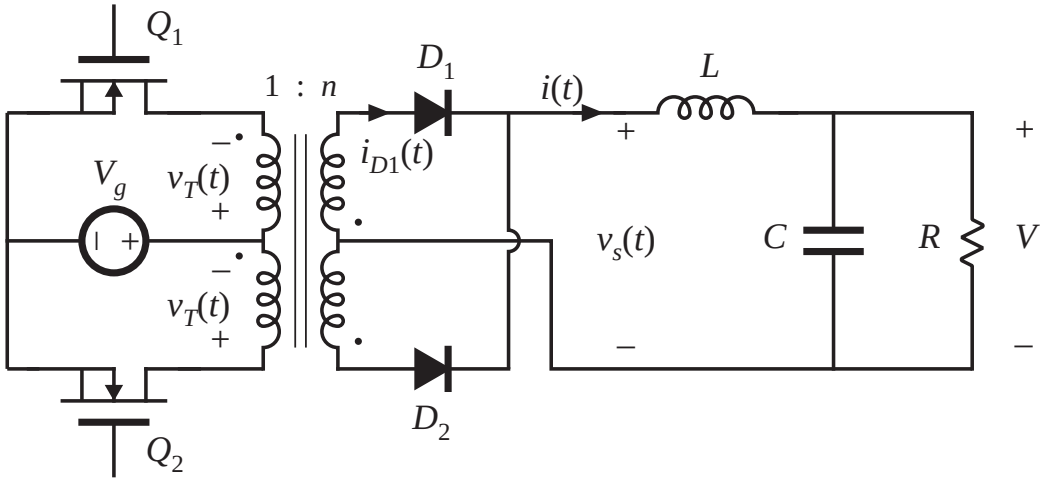
$$D \le \frac{1}{2} \qquad \text{and} \qquad \max(v_{Q1}) = 2V_g$$

The two-transistor forward converter



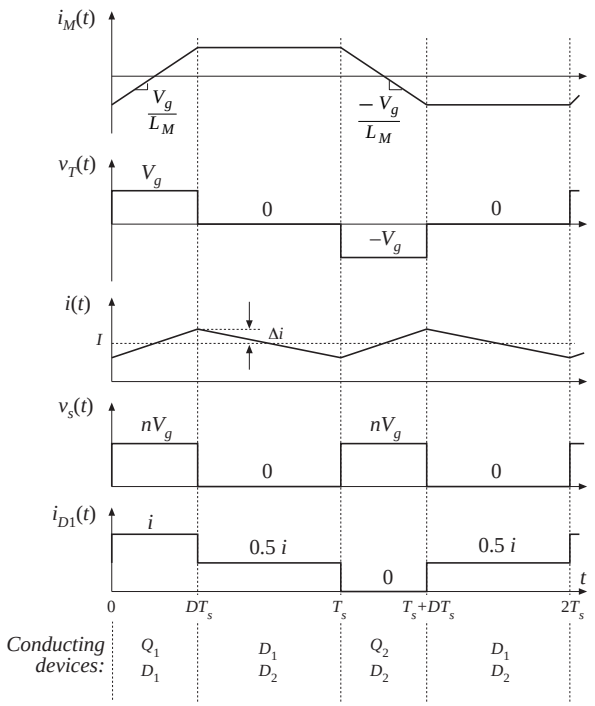
$$V = nDV_g \qquad D \le \frac{1}{2} \qquad \max(v_{Q1}) = \max(v_{Q2}) = V_g$$

6.3.3. Push-pull isolated buck converter



$$V = nDV_g \qquad 0 \le D \le 1$$

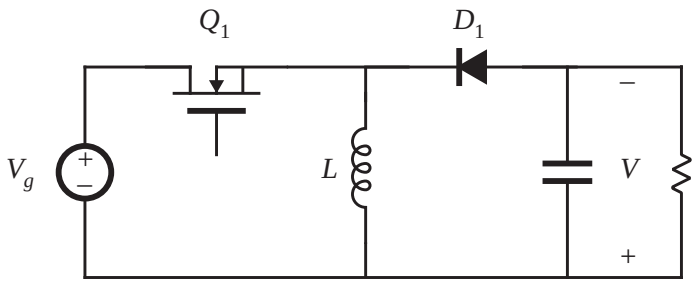
Waveforms: push-pull



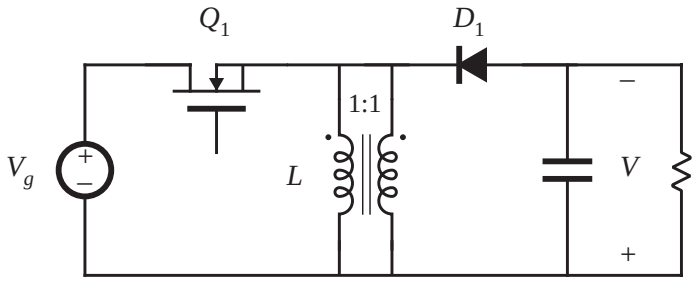
- Used with low-voltage inputs
- Secondary-side circuit identical to full bridge
- As in full bridge, transformer volt-second balance is obtained over two switching periods
- Effect of nonidealities on transformer volt-second balance?
- Current programmed control can be used to mitigate transformer saturation problems. Duty cycle control not recommended.

6.3.4. Flyback converter

buck-boost converter:

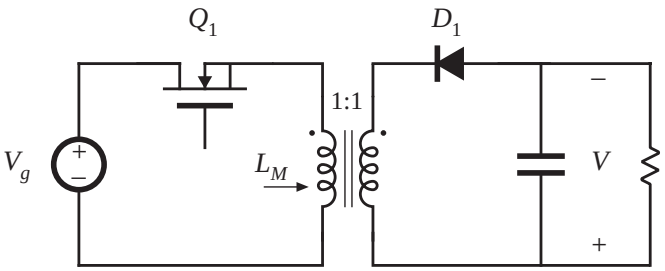


construct inductor winding using two parallel wires:

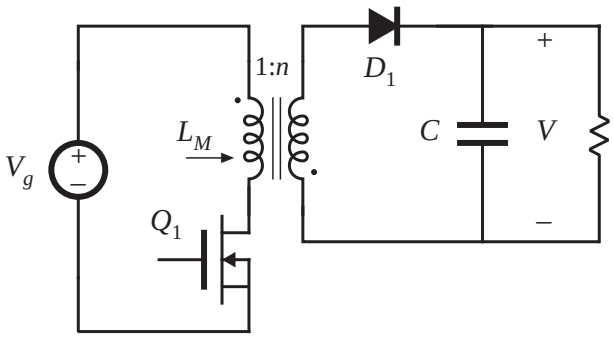


Derivation of flyback converter, cont.

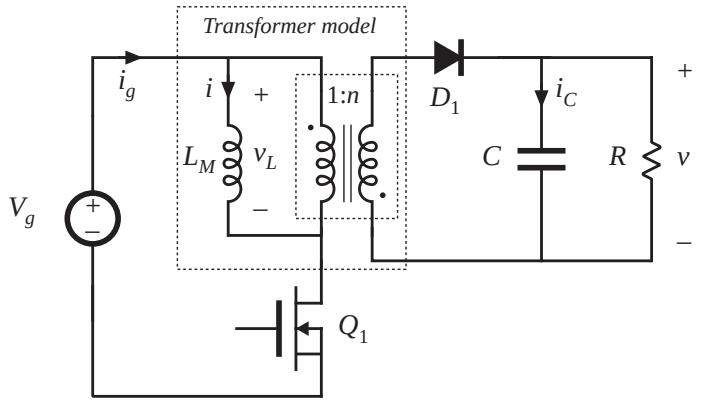
Isolate inductor windings: the flyback converter



Flyback converter having a $1{:}n$ *turns ratio and positive output:*



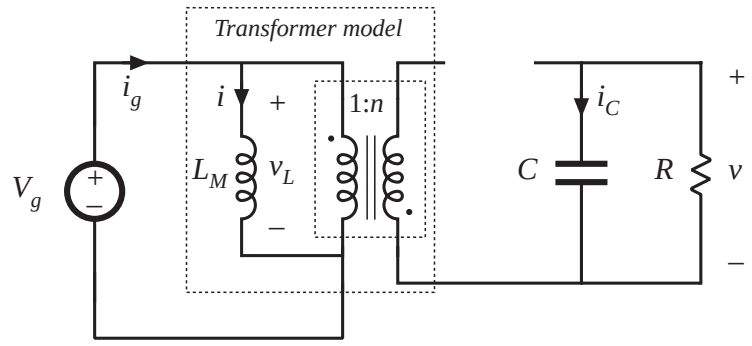
The "flyback transformer"



- A two-winding inductor
- Symbol is same as transformer, but function differs significantly from ideal transformer
- Energy is stored in magnetizing inductance
- Magnetizing inductance is relatively small

- Current does not simultaneously flow in primary and secondary windings
- Instantaneous winding voltages follow turns ratio
- Instantaneous (and rms) winding currents do not follow turns ratio
- Model as (small) magnetizing inductance in parallel with ideal transformer

Subinterval 1



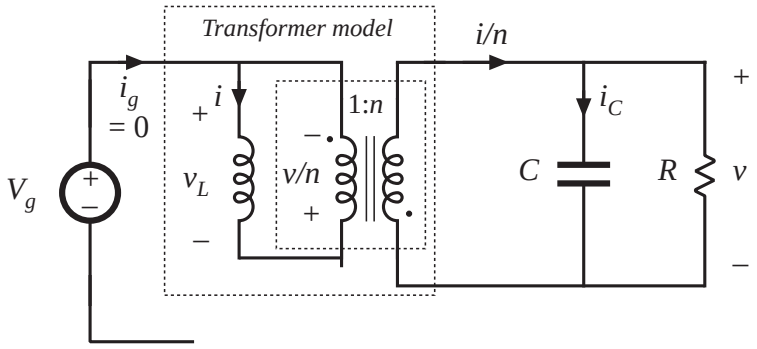
Q_1 on, D_1 off

$$v_L = V_g$$
$$i_C = -\frac{v}{R}$$
$$i_g = i$$

CCM: small ripple approximation leads to

$$v_L = V_g$$
$$i_C = -\frac{V}{R}$$
$$i_g = I$$

Subinterval 2



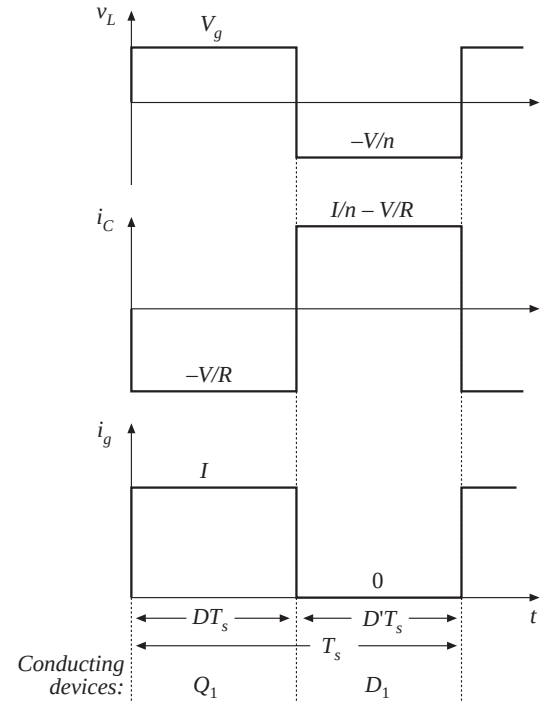
$$v_L = -\frac{v}{n}$$
$$i_C = \frac{i}{n} - \frac{v}{R}$$
$$i_g = 0$$

CCM: small ripple approximation leads to

Q_1 off, D_1 on

$$v_L = -\frac{V}{n}$$
$$i_C = \frac{I}{n} - \frac{V}{R}$$
$$i_g = 0$$

CCM Flyback waveforms and solution



Volt-second balance:

$$\langle v_L \rangle = D\left(V_g\right) + D'\left(-\frac{V}{n}\right) = 0$$

Conversion ratio is

$$M(D) = \frac{V}{V_g} = n\,\frac{D}{D'}$$

Charge balance:

$$\langle i_C \rangle = D\left(-\frac{V}{R}\right) + D'\left(\frac{I}{n} - \frac{V}{R}\right) = 0$$

Dc component of magnetizing current is

$$I = \frac{nV}{D'R}$$

Dc component of source current is

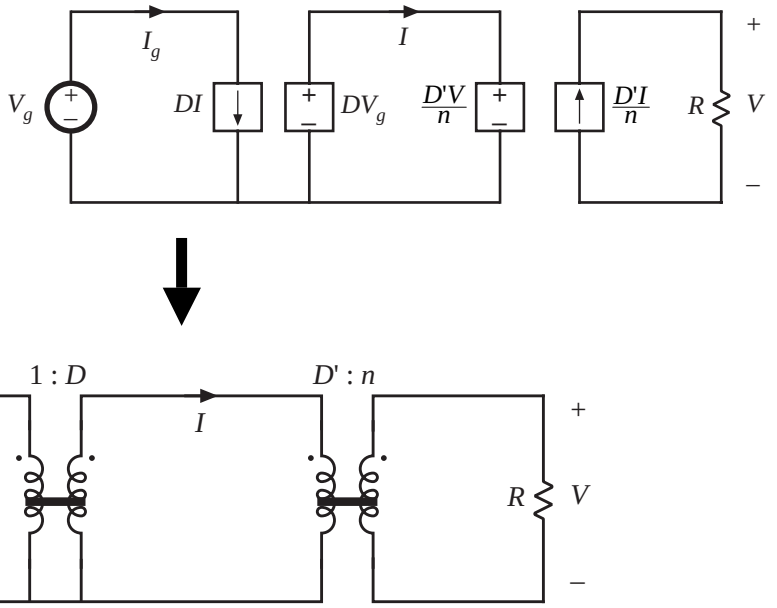
$$I_g = \langle i_g \rangle = D\left(I\right) + D'\left(0\right)$$

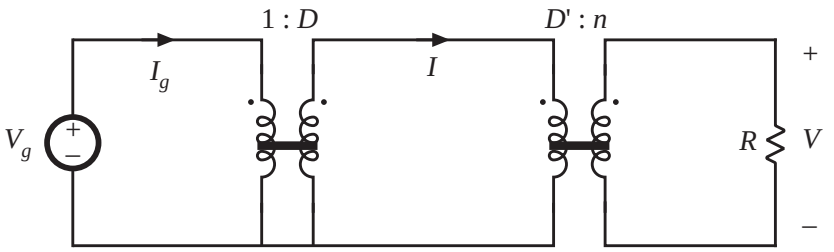
Equivalent circuit model: CCM Flyback

$$\langle v_L \rangle = D\left(V_g\right) + D'\left(-\frac{V}{n}\right) = 0$$

$$\langle i_C \rangle = D\left(-\frac{V}{R}\right) + D'\left(\frac{I}{n} - \frac{V}{R}\right) = 0$$

$$I_g = \langle i_g \rangle = D\left(I\right) + D'\left(0\right)$$





Discussion: Flyback converter

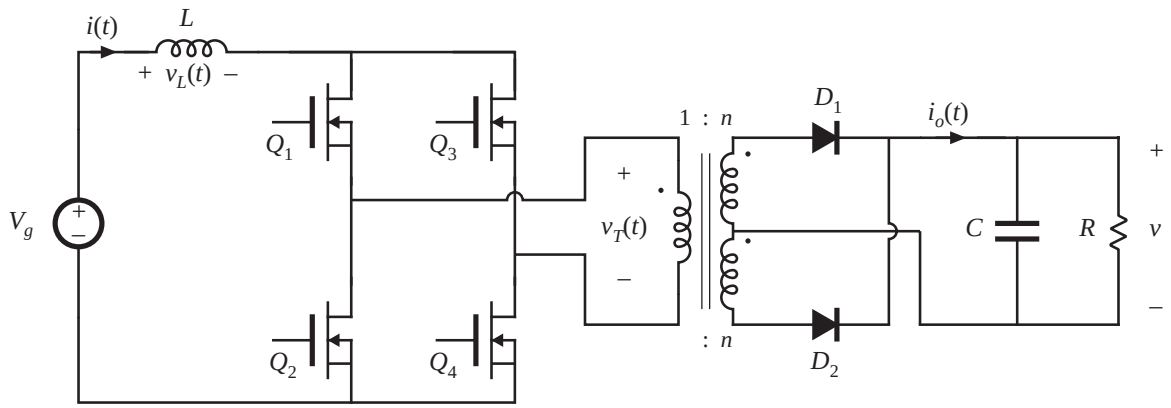
- Widely used in low power and/or high voltage applications
- Low parts count
- Multiple outputs are easily obtained, with minimum additional parts
- Cross regulation is inferior to buck-derived isolated converters
- Often operated in discontinuous conduction mode
- DCM analysis: DCM buck-boost with turns ratio

6.3.5. Boost-derived isolated converters

- A wide variety of boost-derived isolated dc-dc converters can be derived, by inversion of source and load of buck-derived isolated converters:
  - full-bridge and half-bridge isolated boost converters
  - inverse of forward converter: the “reverse” converter
  - push-pull boost-derived converter

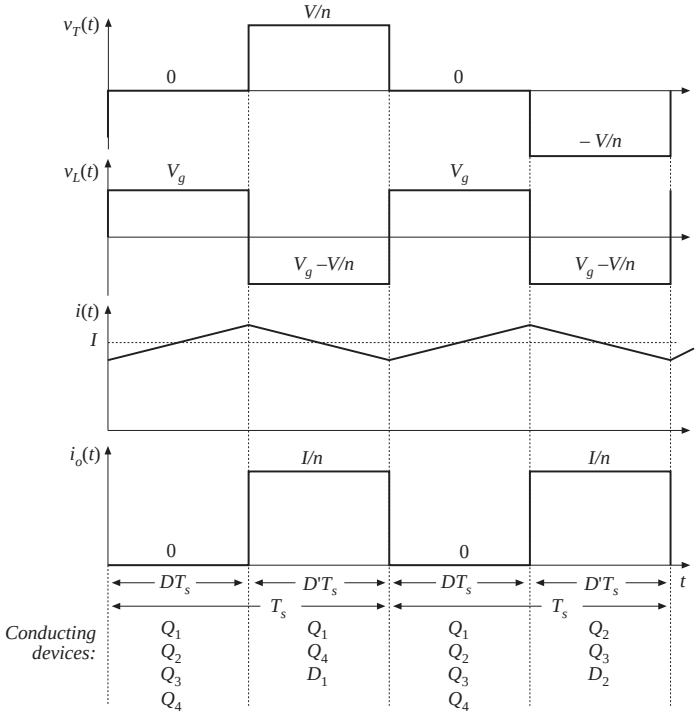
Of these, the full-bridge and push-pull boost-derived isolated converters are the most popular, and are briefly discussed here.

Full-bridge transformer-isolated boost-derived converter



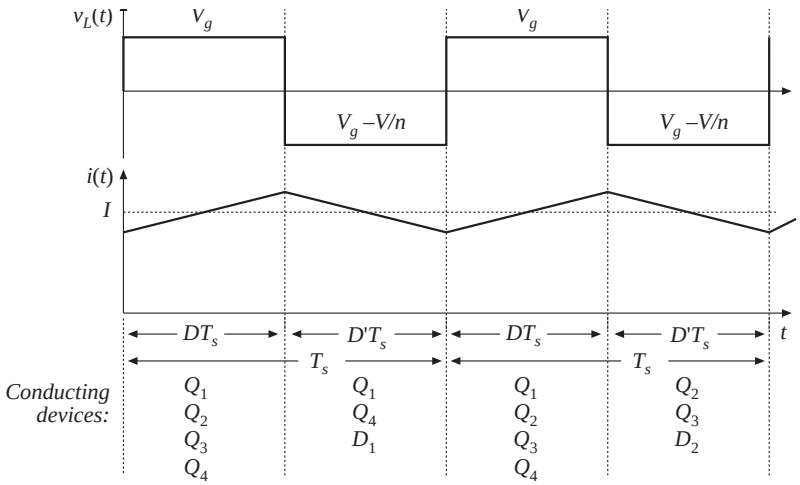
- Circuit topologies are equivalent to those of nonisolated boost converter
- With 1:1 turns ratio, inductor current $i(t)$ and output current $i_o(t)$ waveforms are identical to nonisolated boost converter

Transformer reset mechanism



- As in full-bridge buck topology, transformer volt-second balance is obtained over two switching periods.
- During first switching period: transistors Q_1 and Q_4 conduct for time DT_s , applying volt-seconds VDT_s to secondary winding.
- During next switching period: transistors Q_2 and Q_3 conduct for time DT_s , applying volt-seconds $-VDT_s$ to secondary winding.

Conversion ratio $M(D)$



Application of volt-second balance to inductor voltage waveform:

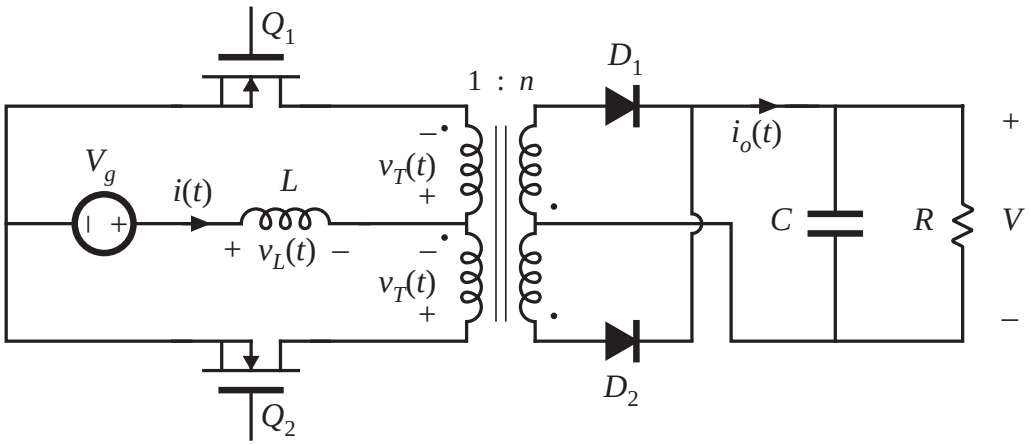
$$\langle v_L \rangle = D\left(V_g\right) + D'\left(V_g - \frac{V}{n}\right) = 0$$

Solve for $M(D)$:

$$M(D) = \frac{V}{V_g} = \frac{n}{D'}$$

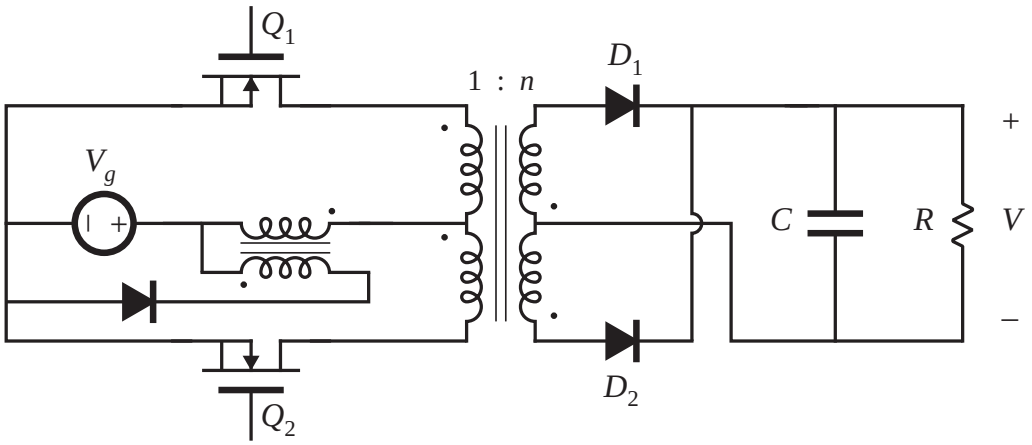
—boost with turns ratio n

Push-pull boost-derived converter



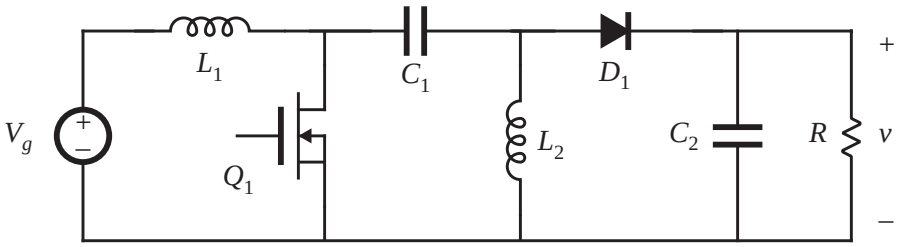
$$M(D) = \frac{V}{V_g} = \frac{n}{D'}$$

Push-pull converter based on Watkins-Johnson converter

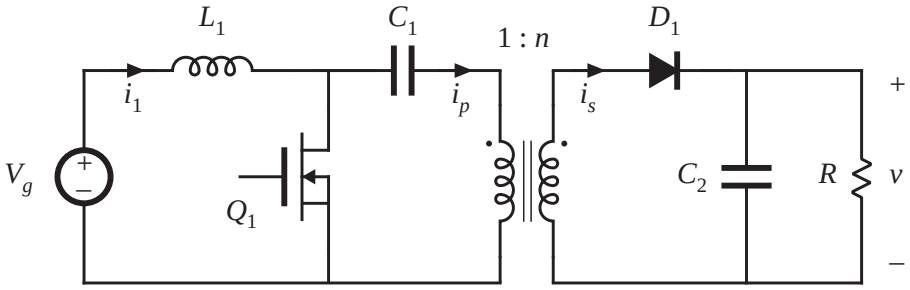


6.3.6. Isolated versions of the SEPIC and Cuk converter

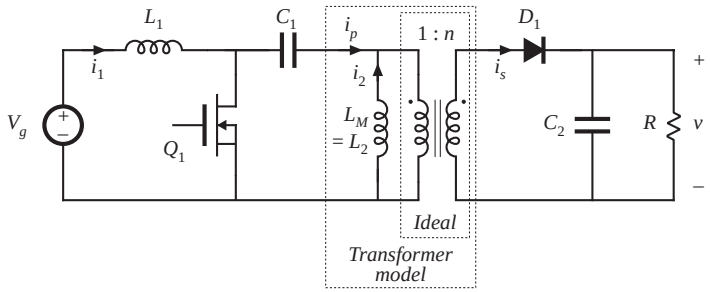
Basic nonisolated SEPIC



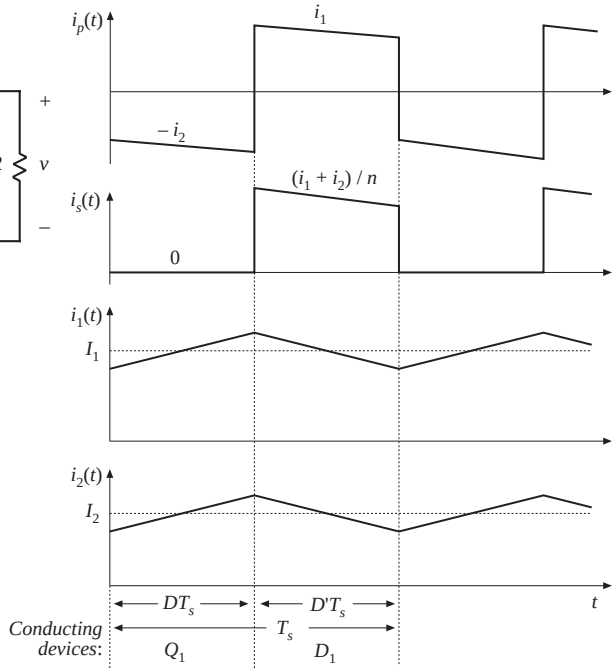
Isolated SEPIC



Isolated SEPIC

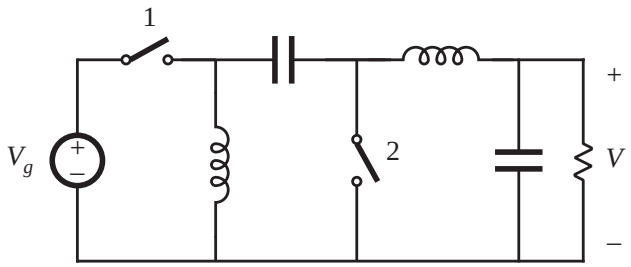


$$M(D) = \frac{V}{V_g} = \frac{nD}{D'}$$

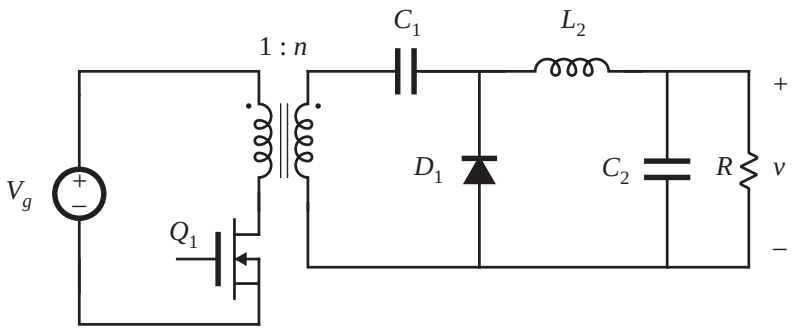


Inverse SEPIC

Nonisolated inverse SEPIC

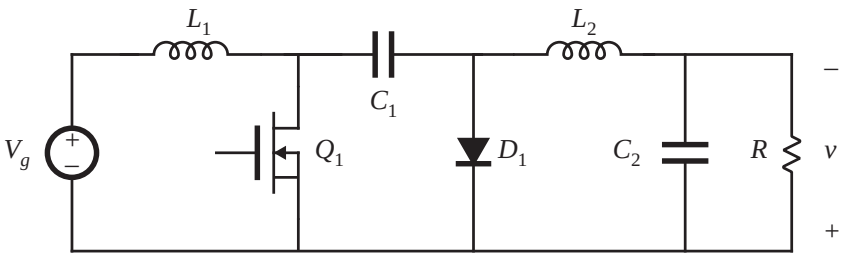


Isolated inverse SEPIC

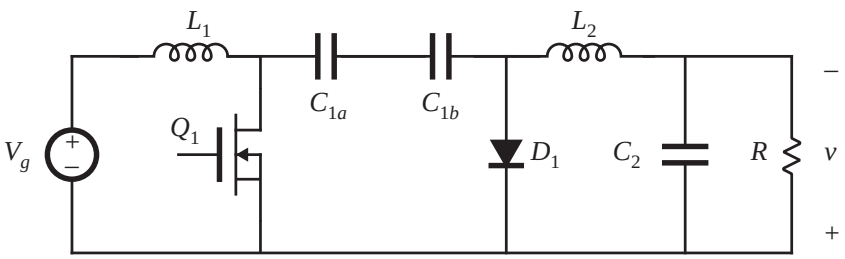


Obtaining isolation in the Cuk converter

Nonisolated Cuk converter



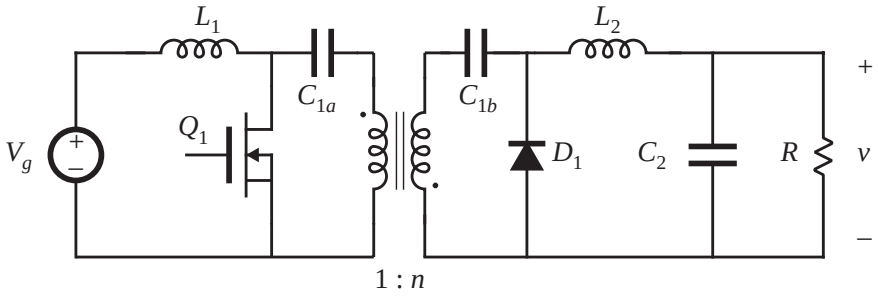
Split capacitor C_1 into series capacitors C_{1a} and C_{1b}



Isolated Cuk converter

Insert transformer between capacitors C_{1a} and C_{1b}

$$M(D) = \frac{V}{V_g} = \frac{nD}{D'}$$



Discussion

- Capacitors C_{1a} *and* C_{1b} ensure that no dc voltage is applied to transformer primary or secondary windings
- Transformer functions in conventional manner, with small magnetizing current and negligible energy storage within the magnetizing inductance

6.4. Converter evaluation and design

For a given application, which converter topology is best?

There is no ultimate converter, perfectly suited for all possible applications

Trade studies

- Rough designs of several converter topologies to meet the given specifications
- An unbiased quantitative comparison of worst-case transistor currents and voltages, transformer size, etc.

Comparison via switch stress, switch utilization, and semiconductor cost

Spreadsheet design

6.4.1. Switch stress and switch utilization

- Largest single cost in a converter is usually the cost of the active semiconductor devices
- Conduction and switching losses associated with the active semiconductor devices often dominate the other sources of loss

This suggests evaluating candidate converter approaches by comparing the voltage and current stresses imposed on the active semiconductor devices.

Minimization of total switch stresses leads to reduced loss, and to minimization of the total silicon area required to realize the power devices of the converter.

Total active switch stress S

In a converter having k active semiconductor devices, the total active switch stress S is defined as

$$S = \sum_{j=1}^{k} V_j I_j$$

where

V_j is the peak voltage applied to switch j,

I_j is the rms current applied to switch j (peak current is also sometimes used).

In a good design, the total active switch stress is minimized.

Active switch utilization U

It is desired to minimize the total active switch stress, while maximizing the output power P_{load}.

The active switch utilization U is defined as

$$U = \frac{P_{load}}{S}$$

The active switch utilization is the converter output power obtained per unit of active switch stress. It is a converter figure-of-merit, which measures how well a converter utilizes its semiconductor devices.

Active switch utilization is less than 1 in transformer-isolated converters, and is a quantity to be maximized.

Converters having low switch utilizations require extra active silicon area, and operate with relatively low efficiency.

Active switch utilization is a function of converter operating point.

CCM flyback example: Determination of S

During subinterval 2, the transistor blocks voltage $V_{Q1,pk}$ equal to V_g plus the reflected load voltage:

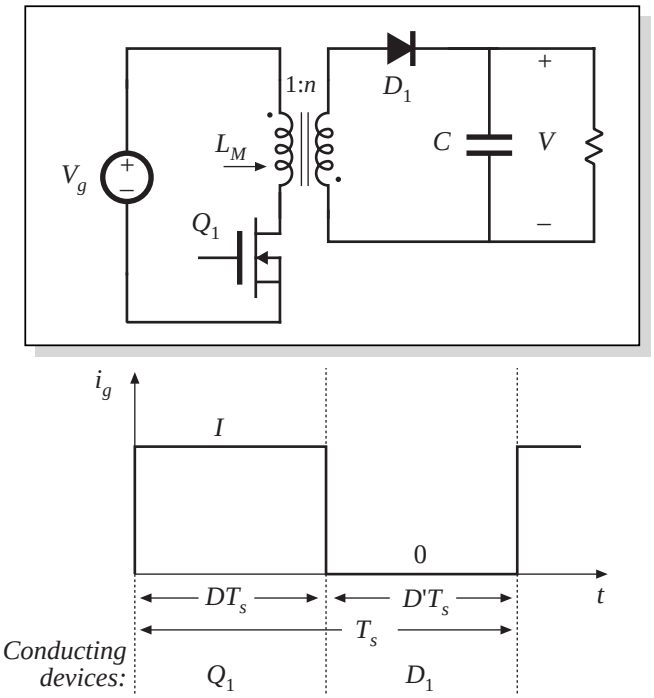
$$V_{Q1,pk} = V_g + \frac{V}{n} = \frac{V_g}{D'}$$

Transistor current coincides with $i_g(t)$. RMS value is

$$I_{Q1,rms} = I\sqrt{D} = \frac{P_{load}}{V_g\sqrt{D}}$$

Switch stress S is

$$S = V_{Q1,pk}\, I_{Q1,rms} = \left(V_g + \frac{V}{n}\right)\left(I\sqrt{D}\right)$$



CCM flyback example: Determination of U

Express load power P_{load} in terms of V and I:

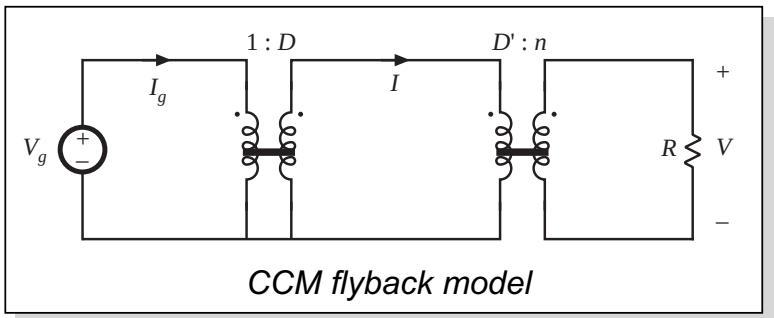
$$P_{load} = D' V \frac{I}{n}$$

Previously-derived expression for S:

$$S = V_{Q1,pk} I_{Q1,rms} = \left(V_g + \frac{V}{n} \right) \left(I \sqrt{D} \right)$$

Hence switch utilization U is

$$U = \frac{P_{load}}{S} = D' \sqrt{D}$$



CCM flyback model

Flyback example: switch utilization $U(D)$

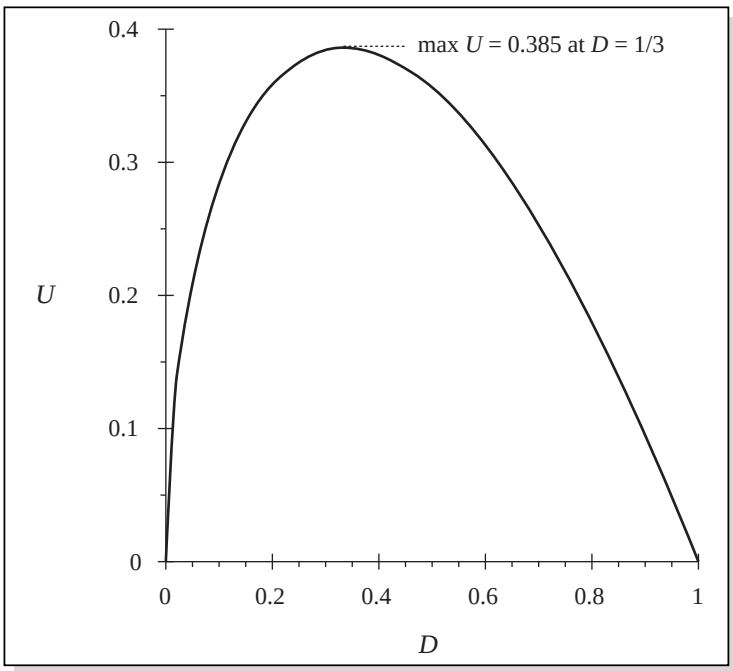
For given V, V_g, P_{load}, the designer can arbitrarily choose D. The turns ratio n must then be chosen according to

$$n = \frac{V}{V_g} \frac{D'}{D}$$

Single operating point design: choose $D = 1/3$.

small D leads to large transistor current

large D leads to large transistor voltage



Comparison of switch utilizations of some common converters

Table 6.1. Active switch utilizations of some common dc-dc converters, single operating point.

Converter	*U(D)*	max *U(D)*	max *U(D)* *occurs at D =*
Buck	$\sqrt{D}$	1	1
Boost	$\frac{D'}{\sqrt{D}}$	∞	0
Buck-boost, flyback, nonisolated SEPIC, isolated SEPIC, nonisolated Cuk, isolated Cuk	$D'\sqrt{D}$	$\frac{2}{3\sqrt{3}} = 0.385$	$\frac{1}{3}$
Forward, $n_1 = n_2$	$\frac{1}{2}\sqrt{D}$	$\frac{1}{2\sqrt{2}} = 0.353$	$\frac{1}{2}$
Other isolated buck-derived converters (full-bridge, half-bridge, push-pull)	$\frac{\sqrt{D}}{2\sqrt{2}}$	$\frac{1}{2\sqrt{2}} = 0.353$	1
Isolated boost-derived converters (full bridge, push-pull)	$\frac{D'}{2\sqrt{1+D}}$	$\frac{1}{2}$	0

Switch utilization : Discussion

- Increasing the range of operating points leads to reduced switch utilization
- Buck converter
  - can operate with high switch utilization (U approaching 1) when D is close to 1
- Boost converter
  - can operate with high switch utilization (U approaching ∞) when D is close to 1
- Transformer isolation leads to reduced switch utilization
- Buck-derived transformer-isolated converters
  - $U \leq 0.353$
  - should be designed to operate with D as large as other considerations allow
  - transformer turns ratio can be chosen to optimize design

Switch utilization: Discussion

- Nonisolated and isolated versions of buck-boost, SEPIC, and Cuk converters

  $U \leq 0.385$

  Single-operating-point optimum occurs at $D = 1/3$

  Nonisolated converters have lower switch utilizations than buck or boost

  Isolation can be obtained without penalizing switch utilization

Active semiconductor cost vs. switch utilization

$$\left(\begin{array}{c}\text{semiconductor cost}\\ \text{per kW output power}\end{array}\right) = \frac{\left(\begin{array}{c}\text{semiconductor device cost}\\ \text{per rated kVA}\end{array}\right)}{\left(\begin{array}{c}\text{voltage}\\ \text{derating}\\ \text{factor}\end{array}\right)\left(\begin{array}{c}\text{current}\\ \text{derating}\\ \text{factor}\end{array}\right)\left(\begin{array}{c}\text{converter}\\ \text{switch}\\ \text{utilization}\end{array}\right)}$$

(semiconductor device cost per rated kVA) = cost of device, divided by product of rated blocking voltage and rms current, in $\$/\text{kVA}$. Typical values are less than $\$1/\text{kVA}$

(voltage derating factor) and (current derating factor) are required to obtain reliable operation. Typical derating factors are 0.5 - 0.75

Typical cost of active semiconductor devices in an isolated dc-dc converter: \$1 - \$10 per kW of output power.

6.4.2. Converter design using computer spreadsheet

Given ranges of V_g and P_{load}, as well as desired value of V and other quantities such as switching frequency, ripple, etc., there are two basic engineering design tasks:

- Compare converter topologies and select the best for the given specifications
- Optimize the design of a given converter

A computer spreadsheet is a very useful tool for this job. The results of the steady-state converter analyses of Chapters 1-6 can be entered, and detailed design investigations can be quickly performed:

- Evaluation of worst-case stresses over a range of operating points
- Evaluation of design tradeoffs

Spreadsheet design example

Specifications

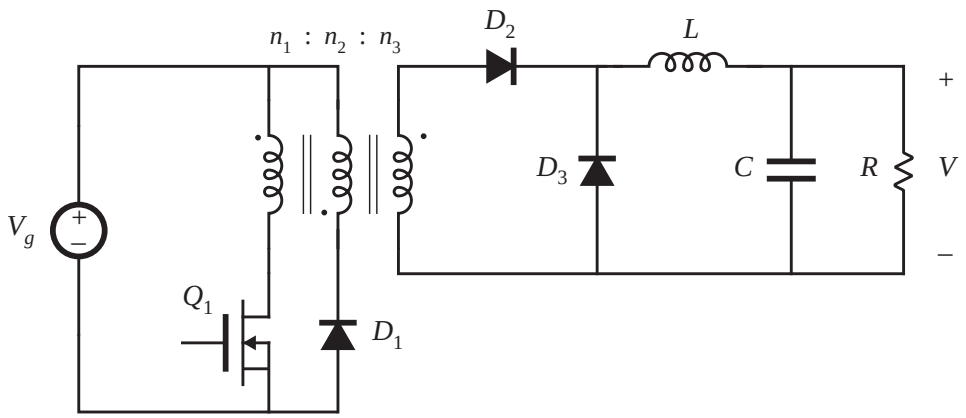
Maximum input voltage V_g	390 V
Minimum input voltage V_g	260 V
Output voltage V	15 V
Maximum load power P_{load}	200 W
Minimum load power P_{load}	20 W
Switching frequency f_s	100 kHz
Maximum output ripple Δv	0.1 V

- Input voltage: rectified 230 Vrms ±20%
- Regulated output of 15 V
- Rated load power 200 W
- Must operate at 10% load
- Select switching frequency of 100 kHz
- Output voltage ripple ≤ 0.1V

Compare single-transistor forward and flyback converters in this application

Specifications are entered at top of spreadsheet

Forward converter design, CCM

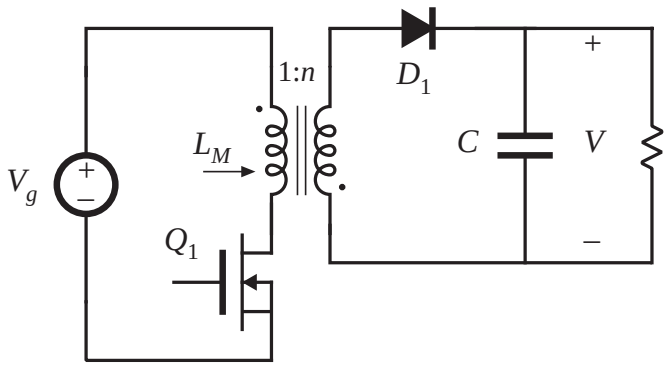


Design variables

Reset winding turns ratio n_2 / n_1	1
Turns ratio n_3 / n_1	0.125
Inductor current ripple Δi	2A ref to sec

- Design for CCM at full load; may operate in DCM at light load

Flyback converter design, CCM



Design variables

Turns ratio n_2 / n_1	0.125
Inductor current ripple Δi	3 A ref to sec

- Design for CCM at full load; may operate in DCM at light load

Enter results of converter analysis into spreadsheet (Forward converter example)

Maximum duty cycle occurs at minimum V_g and maximum P_{load}. Converter then operates in CCM, with

$$D = \frac{n_1}{n_3}\frac{V}{V_g}$$

Inductor current ripple is

$$\Delta i = \frac{D'VT_s}{2L}$$

Solve for L:

$$L = \frac{D'VT_s}{2\Delta i}$$

Δi is a design variable. For a given Δi, the equation above can be used to determine L. To ensure CCM operation at full load, Δi should be less than the full-load output current. C can be found in a similar manner.

Forward converter example, continued

Check for DCM at light load. The solution of the buck converter operating in DCM is

$$V = \frac{n_3}{n_1} V_g \frac{2}{\sqrt{1 + \frac{4K}{D^2}}}$$

with $K = 2L / R T_s$, and $R = V^2 / P_{load}$

These equations apply equally well to the forward converter, provided that all quantities are referred to the transformer secondary side.

Solve for D:

$$D = \frac{2\sqrt{K}}{\sqrt{\left(\frac{2n_3V_g}{n_1V} - 1\right)^2 - 1}} \quad \textit{in DCM} \qquad D = \frac{n_1}{n_3}\frac{V}{V_g} \quad \textit{in CCM}$$

at a given operating point, the actual duty cycle is the small of the values calculated by the CCM and DCM equations above. Minimum D occurs at minimum P_{load} and maximum V_g.

More regarding forward converter example

Worst-case component stresses can now be evaluated.

Peak transistor voltage is

$$\max\left(v_{Q1}\right) = V_g\left(1 + \frac{n_1}{n_2}\right)$$

RMS transistor current is

$$I_{Q1,rms} = \frac{n_3}{n_1}\sqrt{D}\sqrt{I^2 + \frac{\left(\Delta i\right)^2}{3}} \approx \frac{n_3}{n_1}\sqrt{D}\, I$$

(this neglects transformer magnetizing current)

Other component stresses can be found in a similar manner.
Magnetics design is left for a later chapter.

Results: forward and flyback converter spreadsheets

Forward converter design, CCM		***Flyback converter design, CCM***	
Design variables		*Design variables*	
Reset winding turns ratio n_2/n_1	1	Turns ratio n_2/n_1	0.125
Turns ratio n_3/n_1	0.125	Inductor current ripple Δi	3 A ref to sec
Inductor current ripple Δi	2 A ref to sec		
Results		*Results*	
Maximum duty cycle D	0.462	Maximum duty cycle D	0.316
Minimum D, at full load	0.308	Minimum D, at full load	0.235
Minimum D, at minimum load	0.251	Minimum D, at minimum load	0.179
Worst-case stresses		*Worst-case stresses*	
Peak transistor voltage v_{Q1}	780 V	Peak transistor voltage v_{Q1}	510 V
Rms transistor current i_{Q1}	1.13 A	Rms transistor current i_{Q1}	1.38 A
Transistor utilization U	0.226	Transistor utilization U	0.284
Peak diode voltage v_{D2}	49 V	Peak diode voltage v_{D1}	64 V
Rms diode current i_{D2}	9.1 A	Rms diode current i_{D1}	16.3 A
Peak diode voltage v_{D3}	49 V	Peak diode current i_{D1}	22.2 A
Rms diode current i_{D3}	11.1 A		
Rms output capacitor current i_C	1.15 A	Rms output capacitor current i_C	9.1 A

Discussion: transistor voltage

Flyback converter

Ideal peak transistor voltage: 510V

Actual peak voltage will be higher, due to ringing causes by transformer leakage inductance

An 800V or 1000V MOSFET would have an adequate design margin

Forward converter

Ideal peak transistor voltage: 780V, 53% greater than flyback

Few MOSFETs having voltage rating of over 1000 V are available —when ringing due to transformer leakage inductance is accounted for, this design will have an inadequate design margin

Fix: use two-transistor forward converter, or change reset winding turns ratio

A conclusion: reset mechanism of flyback is superior to forward

Discussion: rms transistor current

Forward

1.13A worst-case

transistor utilization 0.226

Flyback

1.38A worst case, 22% higher than forward

transistor utilization 0.284

CCM flyback exhibits higher peak and rms currents. Currents in DCM flyback are even higher

Discussion: secondary-side diode and capacitor stresses

Forward

peak diode voltage 49V

rms diode current 9.1A / 11.1A

rms capacitor current 1.15A

Flyback

peak diode voltage 64V

rms diode current 16.3A

peak diode current 22.2A

rms capacitor current 9.1A

Secondary-side currents, especially capacitor currents, limit the practical application of the flyback converter to situations where the load current is not too great.

Summary of key points

1. The boost converter can be viewed as an inverse buck converter, while the buck-boost and Cuk converters arise from cascade connections of buck and boost converters. The properties of these converters are consistent with their origins. Ac outputs can be obtained by differential connection of the load. An infinite number of converters are possible, and several are listed in this chapter.

2. For understanding the operation of most converters containing transformers, the transformer can be modeled as a magnetizing inductance in parallel with an ideal transformer. The magnetizing inductance must obey all of the usual rules for inductors, including the principle of volt-second balance.

Summary of key points

3. The steady-state behavior of transformer-isolated converters may be understood by first replacing the transformer with the magnetizing-inductance-plus-ideal-transformer equivalent circuit. The techniques developed in the previous chapters can then be applied, including use of inductor volt-second balance and capacitor charge balance to find dc currents and voltages, use of equivalent circuits to model losses and efficiency, and analysis of the discontinuous conduction mode.

4. In the full-bridge, half-bridge, and push-pull isolated versions of the buck and/or boost converters, the transformer frequency is twice the output ripple frequency. The transformer is reset while it transfers energy: the applied voltage polarity alternates on successive switching periods.

Summary of key points

5. In the conventional forward converter, the transformer is reset while the transistor is off. The transformer magnetizing inductance operates in the discontinuous conduction mode, and the maximum duty cycle is limited.
6. The flyback converter is based on the buck-boost converter. The flyback transformer is actually a two-winding inductor, which stores and transfers energy.
7. The transformer turns ratio is an extra degree-of-freedom which the designer can choose to optimize the converter design. Use of a computer spreadsheet is an effective way to determine how the choice of turns ratio affects the component voltage and current stresses.
8. Total active switch stress, and active switch utilization, are two simplified figures-of-merit which can be used to compare the various converter circuits.